APRO Co., Ltd.

SLC Industrial CompactFlash Card

HERMIT-A Series

Product Specification

INDUSTRIAL

CompactFlash Card

Version 01V1

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Revision History

Rev.	***Description***	***Update***
1.0	*Initial release*	*2013/10/1*
1.1	*Add DWPD & TBW Value.*	*2016/07/18*

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1. Introduction

APRO Industrial CompactFlash (CF) Card supports S.M.A.R.T. function – HERMIT Series designed to follow ATAPI-6 (ATA-100) standard. The main used Flash memories are SLC-NAND Type Flash memory chips from 16MB up to 8GB. The operating temperature grade is optional for commercial level 0°C ~ 70°C and wide temperature level -40°C ~ +85°C. The APRO Industrial CompactFlash (CF) Cards supports S.M.A.R.T. function - HERMIT Series are designed electrically complies with the conventional IDE hard Card and support True IDE Mode. The data transfer modes supports PIO mode 0, 1, 2, 3, 4 or MWDMA- 0, 1, 2 or UDMA- 0, 1, 2, 3, 4. The fastest reading speed is up to 37.8 MB/sec and writing speed is up to 27.0 MB/sec. In order to sustain various harsh and tough operating environments, APRO especially delivers the CompactFlash frame kit in rugged metal as well as provides the optional treatment of conformal coating upon customers' request.

The APRO Industrial CF card products provide a high level interface to the host computer. This interface allows a host computer to issue commands to the CompactFlash (CF) Card to read or write blocks of memory. Each sector is protected by a powerful 4 bits Error Correcting Code (ECC). APRO Industrial CompactFlash (CF) Card's HERMIT Series intelligent controller manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech Industrial CompactFlash (CF) Card controller.

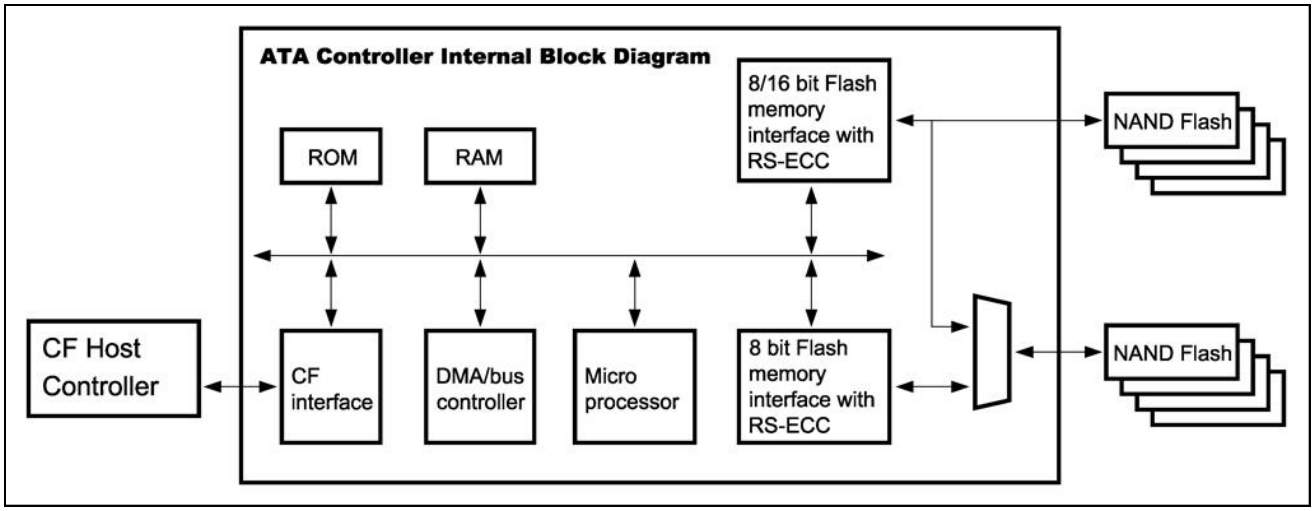


Figure 1: CompactFlash Card HERMIT Series Controller Block Diagram

1.1. *Scope*

This document describes the features and specifications and installation guide of APRO's Industrial CF Cards supports S.M.A.R.T. function – HERMIT Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. *System Features*

- Optional Rugged metal CompactFlash casing to sustain the harshest environments
- SLC-NAND type flash technology
- Card capacity from 16MB to 8GB
- Supports S.M.A.R.T. function (Self-Monitoring, Analysis and Reporting Technology)
- ATA inter face and support PC Card Memory mode, PC Card I/O mode and True IDE mode
- Data transfer supports PIO-6 and UDMA-4 (Default setting)
- Sequential read : 37.8 MB/sec; Write: 27.0MB/sec. (1GB, max.)
- Automatic 4 bits error correction (ECC) and retry capabilities
- +5 V ±10% or +3.3 V ±5% operation
- MTBF 3,000,000 hours.
- Shock : 1,500G , compliance to MIL-STD-810F
- Vibration : 15G, compliance to MIL-STD-810F
- Work well in severe environments
- Very high performance, very low power consumption
- Low weight, Noiseless
- Conformal coating upon special request

1.3. *CFA 3.0 Specification*

APRO Industrial CF card – HERMIT Series is fully compatible with the CFA 3.0 specification.

1.4. *ATA/ATAPI-6 Standard*

APRO Industrial CF card – HERMIT Series is compliant to ATA/ATAPI-6 and below version.

1.5. *Technology Independence - Static Wear Leveling*

In order to gain the best management for flash memory, APRO Industrial CF card – HERMIT Series supports Static Wear Leveling technology to manage the Flash system. The life of flash memory is limited; the management is to increase the life of the flash product.

A static wear-leveling algorithm evenly distributes data over an entire Flash cell array and searches for the least used physical blocks. The identified low cycled sectors are used to write the data to those locations. If blocks are empty, the write occurs normally. If blocks contain static data, it moves that data to a more heavily used location before it moves the newly written data. The static wear leveling maximizes effective endurance Flash array compared to no wear leveling or dynamic wear leveling.

1.6. *Conformal coating*

Conformal coating is a protective, dielectric coating designed to conform to the surface of an assembled printed circuit board. Commonly used conformal coatings include silicone, acrylic, urethane and epoxy. APRO applies only silicone on APRO storages products upon requested especially by customers. The type of silicone coating features good thermal shock resistance due to flexibility. It is also easy to apply and repair.

Conformal coating offers protection of circuitry from moisture, fungus, dust and corrosion caused by extreme environments. It also prevents damage from those Flash storages handling during construction, installation and use, and reduces mechanical stress on components and protects from thermal shock. The greatest advantage of conformal coating is to allow greater component density due to increased dielectric strength between conductors.

APRO uses MIL-I-46058C silicon conformal coating.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 1: Environmental Specification

APRO Industrial CF card - HERMIT Series		Commercial Grade	Industrial Grade
Temperature	**Operating:**	0ºC ~ +70ºC	-40ºC ~ +85ºC
	Non-operating:	-20ºC ~ +80ºC	-50ºC ~ +95ºC
Humidity	**Operating & Non-operating:**	10% ~ 95% non-condensing	
Vibration	**Operating & Non-operating:**	15G compliance to MIL-STD-810F	
Shock	**Operating & Non-operating:**	1,500G compliance to MIL-STD-810F	
Altitude	**Operating & Non-operating:**	70,000 feet	

2.2. System Power Requirements

Table 2: Power Requirement

APRO Industrial CF card - HERMIT Series	Commercial Grade	Industrial Grade
DC Input Voltage (VCC)	5V±10% or 3.3V±5%	
Reading mode	124 mA (Max)	
Writing mode	121 mA (Max)	
Idle mode	1.8 mA (Max)	

2.3. System Performance

Table 3: System Performances

Data Transfer Mode supporting			- PIO mode : 0, 1, 2, 3, 4, 5 ,**6**,**(PIO – 6 defaulted)** - DMA SW Mode: Not supported - DMA MW Mode:0,1, 2 - UDMA Mode: 0,1,2,3, **4 (UDMA-4 defaulted)**								
Data Transfer Rate To/From Host			16.6Mybtes/sec burst under PIO Mode 4 as defaulted 66.6Mbytes/sec burst under UDMA-4 Mode as defaulted								
Average Access Time			0.2 ms(estimated)								
Maximum Performance	**Capacity**		16MB	32MB	64MB	128MB	256MB	512MB	1GB	2GB	4GB	8GB
	Sequential Read (MB/s)	**PIO- 6**	4.0	4.0	4.0	4.0	4.0	4.0	4.7	4.7	4.7	4.6
		UDMA -4	17.15	17.15	17.41	17.8	17.8	19.8	37.8	36.7	36.5	38.29
	Sequential Write(MB/s)	**PIO- 6**	4.2	4.2	4.2	4.2	4.2	4.0	4.6	4.6	4. 6	4.0
		UDMA -4	5.94	5.94	6.02	11.2	11.2	13.7	27.0	26.4	26.6	16.59
The number of Channel			Single	Single	Single	Single	Single	Single	Dual	Dual	Dual	Dual

Note:

(1). All values quoted are typically at 25℃ and nominal supply voltage.

(2). Testing of the Industrial CompactFlash (CF) Card maximum performance was performed under the following platform:

- Computer with AMD 3.0GHz processor

- Windows XP Professional operating system

(3). Above performance data are for reference only for the performance would be different for various factors such like flash memory chips, system configuration and software for performance testing,…etc.

2.4. *System Reliability*

Table 4: System Reliability

MTBF	3,000,000 hours	
Wear-leveling Algorithms	Static wear-leveling algorithms	
ECC Technology	4 bits per 512 bytes block	
Erase counts	NAND SLC Flash Cell Level : 60K P/E Cycles	
Data Retention	10 years	
Capacity	**TBW(TB)**	**DWPD & Lifespan**
16MB	0.8	Lifespan = 5 Years; DWPD=29.62 DWPD (Disk Written Per Day)
32MB	1.7	
64MB	3.3	
128MB	6.58	
256MB	13.18	
512MB	26.36	
1GB	52.73	
2GB	105.46	
4GB	210.9	
8GB	421.8	

2.5. *Physical Specifications*

Refer to Table 5 and see Figure 2 for Industrial CF HERMIT Series physical specifications and dimensions.

Table 5: Physical Specifications

Industrial CompactFlash Card (Type I CompactFlash)	
Length:	36.40±0.15mm(1.433±0.006 in)
Width:	42.80±0.10mm(1.685±0.004 in)
Thickness:	3.3mm±0.10mm(.130±0.004 in) (Excluding Lip)
Weight:	12.0g(0.42oz) typical, 14.2 g (.0.5 oz) maximum

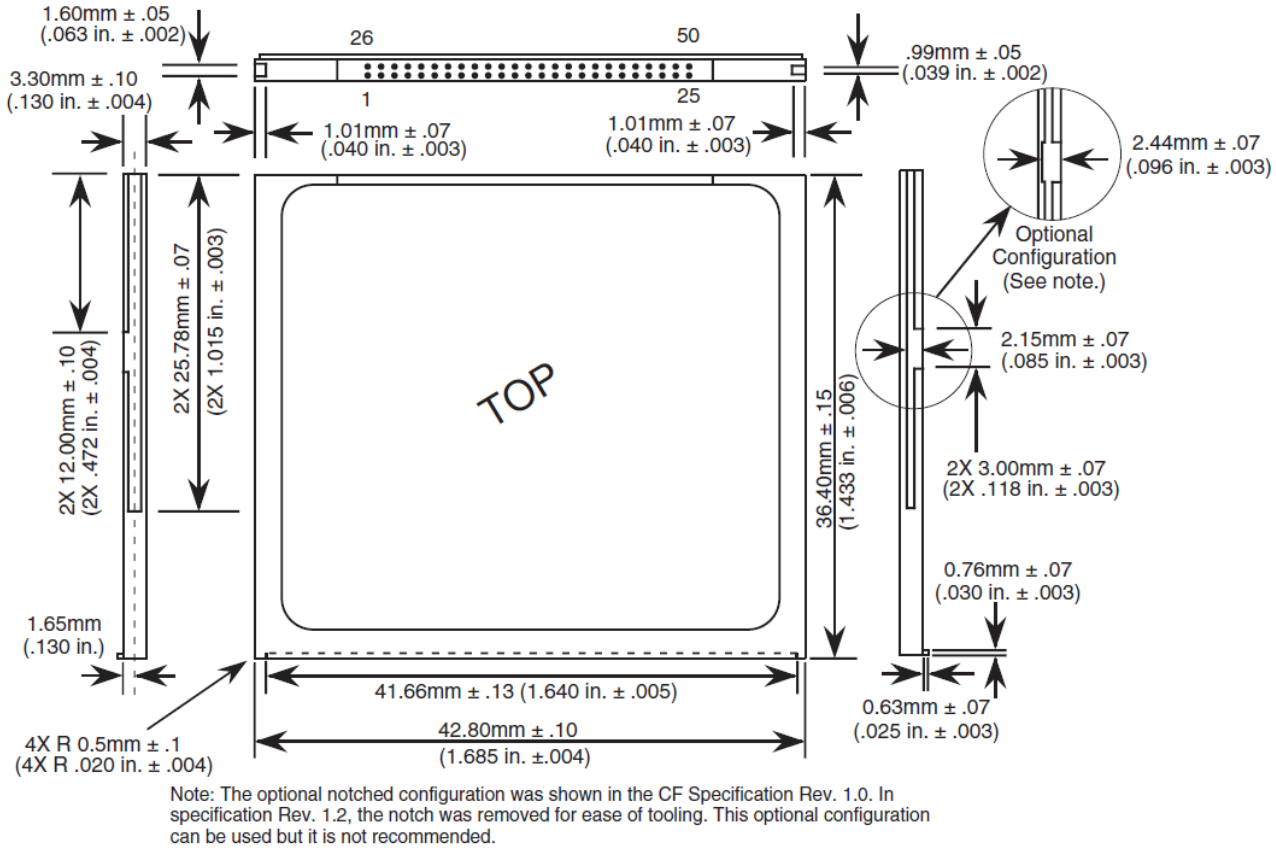


Figure 2: CompactFlash Card Dimension

2.6. *Capacity Specifications*

The table 6 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 6: Device Parameter

Unformatted Capacity	Default Cylinder	Default Head	Default Sector	LBA Total Sectors
16MB	248	4	32	31,744
32MB	500	8	16	64,000
64MB	500	8	32	112,000
128MB	480	16	32	245,760
256MB	984	16	32	503,808
512MB	1,001	16	63	1,009,008
1GB	2,002	16	63	2,018,016
2GB	4,003	16	63	4,035,024
4GB	8,006	16	63	8,070,048
8GB	16,000	16	63	16,128,000

3. Interface Description

3.1. CF interface (CompactFlash Type I)

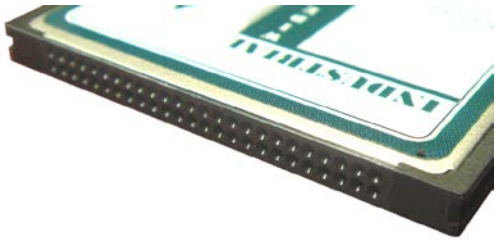


Figure 3: 50-pin CompactFlash Type I Connector

3.2. Pin Assignments

Signals whose source is the host is designated as inputs while signals that the Industrial CompactFlash (CF) Card sources are outputs. The pin assignments are listed in below table 7.

The signal/pin assignments are listed in below Table 7. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output.

Table 7: Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	11Z,OZ3	2	D03	I/O	11Z,OZ3	2	D03	I/O	11Z,OZ3
3	D04	I/O	11Z,OZ3	3	D04	I/O	11Z,OZ3	3	D04	I/O	11Z,OZ3
4	D05	I/O	11Z,OZ3	4	D05	I/O	11Z,OZ3	4	D05	I/O	11Z,OZ3
5	D06	I/O	11Z,OZ3	5	D06	I/O	11Z,OZ3	5	D06	I/O	11Z,OZ3
6	D07	I/O	11Z,OZ3	6	D07	I/O	11Z,OZ3	6	D07	I/O	11Z,OZ3
7	-CE1	I	13U	7	-CE1	I	13U	7	-CS0	I	13Z
8	A10	I	11Z	8	A10	I	11Z	8	A10[2]	I	11Z
9	-OE	I	13U	9	-OE	I	13U	9	-ATA SEL	I	13U
10	A09	I	11Z	10	A09	I	11Z	10	A09[2]	I	11Z
11	A08	I	11Z	11	A08	I	11Z	11	A08[2]	I	11Z
12	A07	I	11Z	12	A07	I	11Z	12	A07[2]	I	11Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	11Z	14	A06	I	11Z	14	A06[2]	I	11Z
15	A05	I	11Z	15	A05	I	11Z	15	A05[2]	I	11Z
16	A04	I	11Z	16	A04	I	11Z	16	A04[2]	I	11Z
17	A03	I	11Z	17	A03	I	11Z	17	A03[2]	I	11Z
18	A02	I	11Z	18	A02	I	11Z	18	A02	I	11Z
19	A01	I	11Z	19	A01	I	11Z	19	A01	I	11Z

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type
20	A00	I	11Z	20	A00	I	11Z	20	A00	I	11Z
21	D00	I/O	11Z,OZ3	21	D00	I/O	11Z,OZ3	21	D00	I/O	11Z,OZ3
22	D01	I/O	11Z,OZ3	22	D01	I/O	11Z,OZ3	22	D01	I/O	11Z,OZ3
23	D02	I/O	11Z,OZ3	23	D02	I/O	11Z,OZ3	23	D02	I/O	11Z,OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	11Z,OZ3	27	D11[1]	I/O	11Z,OZ3	27	D11[1]	I/O	11Z,OZ3
28	D12[1]	I/O	11Z,OZ3	28	D12[1]	I/O	11Z,OZ3	28	D12[1]	I/O	11Z,OZ3
29	D13[1]	I/O	11Z,OZ3	29	D13[1]	I/O	11Z,OZ3	29	D13[1]	I/O	11Z,OZ3
30	D14[1]	I/O	11Z,OZ3	30	D14[1]	I/O	11Z,OZ3	30	D14[1]	I/O	11Z,OZ3
31	D15[1]	I/O	11Z,OZ3	31	D15[1]	I/O	11Z,OZ3	31	D15[1]	I/O	11Z,OZ3
32	-CE2[1]	I	13U	32	-CE2[1]	I	13U	32	-CS1[1]	I	13Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD	I	13U	34	-IORD	I	13U	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I	13Z
35	-IOWR	I	13U	35	-IOWR	I	13U	35	-IOWR[7] STOP[8,9]	I	13Z
36	-WE	I	13U	36	-WE	I	13U	36	-WE[3]	I	13U
37	READY	O	OT1	37	-IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL[5]	I	12Z	39	-CSEL[5]	I	12Z	39	-CSEL	I	12U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	12Z	41	RESET	I	12Z	41	-RESET	I	12Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY[7] -DDMARDY[8] DSTROBE[9]	O	ON1
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	DMARQ	O	OZ1
44	-REG	I	13U	44	-REG	I	13U	44	-DMACK[6]	I	13U
45	BVD2	O	OT1	45	-SPKR	O	OT1	45	-DASP	I/O	11U,ON1

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type
46	BVD1	O	OT1	**46**	-STSCHG	O	OT1	**46**	-PDIAG	I/O	11U.ON1
47	D08[1]	I/O	11Z,OZ3	**47**	D08[1]	I/O	11Z,OZ3	**47**	D08[1]	I/O	11Z,OZ3
48	D09[1]	I/O	11Z,OZ3	**48**	D09[1]	I/O	11Z,OZ3	**48**	D09[1]	I/O	11Z,OZ3
49	D10[1]	I/O	11Z,OZ3	**49**	D10[1]	I/O	11Z,OZ3	**49**	D10[1]	I/O	11Z,OZ3
50	GND		Ground	**50**	GND		Ground	**50**	GND		Ground

Note:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.

2) The signal should be grounded by the host.

3) The signal should be tied to VCC by the host.

4) The mode is optional for CF+ Cards, but required for CompactFlash Cards.

5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.

6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition

7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.

8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.

9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

3.3. *Electrical Description*

The APRO Industrial CompactFlash Card -HERMIT Series is optimized for operation with hosts, which support the PCMCIA/ I/O interface standard conforming to the PC Card ATA specification. However, the CompactFlash Card may also be configured to operate in systems that support only the memory interface standard. The configuration of the CompactFlash Card will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the CompactFlash Card.

Table 8: describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the CompactFlash Card sources are outputs. The CompactFlash Card logic levels conform to those specified in the *PCMCIA Release 2.1 Specification*. See Section 3.3 for definitions of Input and Output type.

Table 8: Signal Description

Signal Name	Dir	Pin	Description
A10 – A0 (PC Card Memory Mode) A10 – A0 (PC Card I/O Mode)	I	8,10,11,12,14, 15,16,17,18,19 ,20	These address lines along with the –REG signal are used to select the following : The I/O port address registers within the CompactFlash Card or CF+ Card, the memory mapped port address registers within the CompactFlash Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal.
A2 – A0 (True IDE Mode)	I	18,19,20	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode) -STSCHG (PC Card I/O Mode) Status Changed -PDIAG (True IDE Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported. This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. It use is controlled by the Card Config and Status Register. In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode) -SPKR (PC Card I/O Mode) -DASP (True IDE Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported. This line is the Binary Audio output from t he card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Card or CF+ Card. They are used by the host to determine that the CompactFlash Card or CF+ Card is fully inserte4d into its socket.

Signal Name	Dir	Pin	Description
-CD1, -CD2 (PC Card I/O Mode) -CD1, -CD2 (True IDE Mode)			This signal is the same for all modes. This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable -CE1, -CE2 (PC Card I/O Mode) Card Enable -CS0, -CS1 (True IDE Mode)	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, -CS0 is the chip select for the task file registers while –CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16bits.
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode)	I	39	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When the pin is open, this device is configured as a Slave.
D15 – D00 (PC Card Memory Mode) D15 – D00 (PC Card I/O Mode) D15 – D00 (True IDE Mode)	I/O	31,30,29,28,27 ,49,48,47,6,5,4 ,3,2,23,22,21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode) GND (PC Card I/O Mode) GND	--	1,50	Ground This signal is the same for all modes. This signal is the same for all modes.

Signal Name	Dir	Pin	Description
(True IDE Mode)			
-INPACK (PC Card Memory Mode) -INPACK (PC Card I/O Mode) Input Acknowledge DMARQ (True IDE Mode)	O	43	This signal is not used in this mode. The Input Acknowledge signal is asserted by the CompactFlash Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Card or CF+ Card and the CPU. This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. This signal is used in a handshake manner with –DMACK, i.e., the device shall wait until the host asserts –DMACK before negating DMARQ, and re-asserting DMARQ if there is more data to transfer. DMAARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode) -IORD (PC Card I/O Mode) -IORD (True IDE Mode –Except Ultra DMA Protocol Active) -HDMARDY (True IDE Mode – In Ultra DMA Protocol	I	34	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Card or CF+ Card when the card is configured to use the I/O interface. In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode. In True IDE Mode when Ultra DMA mode DMA Read is active this signal is asserted by the host to indicate that the host is read to receive Ultra DMA

Signal Name	Dir	Pin	Description
DMA Read) HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			data-in bursts. The host may negate –HDMARDY to pause an Ultra DMA transfer. In True IDE Mode when Ultra DMA mode DMA Write is active this signal is the data out strobe generated by the host. Both rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
-IOWR (PC Card Memory Mode) -IOWR (PC Card I/O Mode) -IOWR (True IDE Mode – Except Ultra DMA Protocol Active) STOP (True IDE Mode – Ultra DMA Protocol Active)	I	35	This signal is not used in this mode. The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Card or CF+ Card controller registers when the CompactFlash Card or CF+ Card is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge). In True IDE Mode, while Ultra DMA mode protocol is not active this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol. In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
-OE (PC Card Memory Mode) -OE (PC Card I/O Mode) -ATA SEL (True IDE Mode)	I	9	This is an Output Enable Strobe Generated by the host interface. It is used to read data from the CompactFlash Card or CF+ Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode this input should be grounded by the host.
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy. At power up and at Reset, the READY signal is held low (bus) until the CompactFlash Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Card or CF+ Card during this time. Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET

Signal Name	Dir	Pin	Description
-IREQ (PC Card I/O Mode) INTRQ (True IDE Mode)			pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state. I/O Operation – After the CompactFlash Card or CF+ Card has been configured for I/O operation, this signal is used as –Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level ode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select -REG (PC Card I/O Mode) -DMACK (True IDE Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus. This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the –DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long a this does not prevent proper operation all modes.
RESET (PC Card Memory Mode) RESET (PC Card I/O Mode) -RESET (True IDE Mode)	I	41	The CompactFlash Card or CF+ Card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The CompactFlash Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode, this input pin is the active low hardware reset from the host.

Signal Name	Dir	Pin	Description
VCC (PC Card Memory Mode) VCC (PC Card I/O Mode) VCC (True IDE Mode)	--	13,38	+5V, +3.3V power. This signal is the same for all modes. This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode) -VS1 -VS2 (PC Card I/O Mode) -VS1 -VS2 (True IDE Mode)	O	33 40	Voltage Sense Signals. –VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Card or CF+ Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card. This signal is the same for all modes. This signal is the same for all modes.
-WAIT (PC Card Memory Mode) -WAIT (PC Card I/O Mode) IORDY (True IDE Mode –Except Ultra DMA Mode) -DDMARDY (True IDE Mode –Ultra DMA Write Mode) DSTROBE (True IDE Mode –Ultra DMA Read Mode)	O	42	The –WAIT signal is driven low by the CompactFlash Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY. In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate –DDMARDY to pause an Ultra DMA transfer. In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.

Signal Name	Dir	Pin	Description
-WE (PC Card I/O Mode) -WE (True IDE Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect -IOIS16 (PC Card I/O Mode) -IOIS16 (True IDE Mode)	O	24	Memory Mode –The CompactFlash Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation –When the CompactFlash Card or CF+ Card is configured for I/O Operation Pin 24 is used for the –I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

4. Electrical Specification

Table 9, Table 10, and Table 11 defines all D.C. Characteristics for the Industrial CompactFlash (CF) Card. Unless otherwise stated, a condition is as below Table 9:

Table 9: Electrical Condition

Commercial Grade	Industrial Grade
Vcc = 5V ±10%	Vcc = 5V ±10%
Vcc = 3.3V ± 10%	Vcc = 3.3V ± 10%
Ta = 0°C to 70°C	Ta = -40°C to 85°C

4.1. *General DC Characteristics*

4.1.1. Interface I/O at 5.0V

Table 10: Interface I/O at 5.0V

Symbol	Parameter	Min.	Max.	Units	Remark
V_{CC}	Power Supply	4.5	5.5	V	
V_{OH}	Output Voltage High Level	VCC-0.8		V	
V_{OL}	Output Voltage Low Level		0.8	V	
V_{IH}	Input Voltage High Level	2.92		V	Schmitt trigger[1]
V_{IL}	Input Voltage Low Level		1.70	V	Schmitt trigger[1]
T_{OPR-W}	Operating temperature for wide grade	-40	+85	℃	
T_{OPR-S}	Operating temperature for standard grade	0	+70	℃	
T_{STG}	Storage temperature	-40	125	℃	

R_{PU}	Pull up resistance[2]	50	73	kOhm	
R_{PD}	Pull down resistance	50	97	kOhm	

4.1.2. Interface I/O at 3.3V

Table 11: Interface I/O at 3.3V

Symbol	Parameter	Min.	Max.	Units	Remark
V_{OH}	Power Supply	2.97	3.63	V	
V_{OL}	Output Voltage High Level	VCC-0.8		V	
V_{IH}	Output Voltage Low Level		0.8	V	
V_{IL}	Input Voltage High Level	2.05		V	Schmitt trigger[1]
V_{CC}	Input Voltage Low Level		1.25	V	Schmitt trigger[1]
T_{OPR-W}	Operating Temperature For Wide Grade	-40	+85	℃	
T_{OPR-S}	Operating Temperature For Standard Grade	0	+70	℃	
T_{STG}	Storage Temperature	-40	125	℃	
R_{PU}	Pull up resistance2	52.7	141	kOhm	
R_{PD}	Pull down resistance	47.5	172	kOhm	

Notes:

1) *Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW pins.*

2) *Include CE1, CE2, HREG, HOE, HIOE, HWE, HIOW, CSEL, PDIAG, DASP pins.*

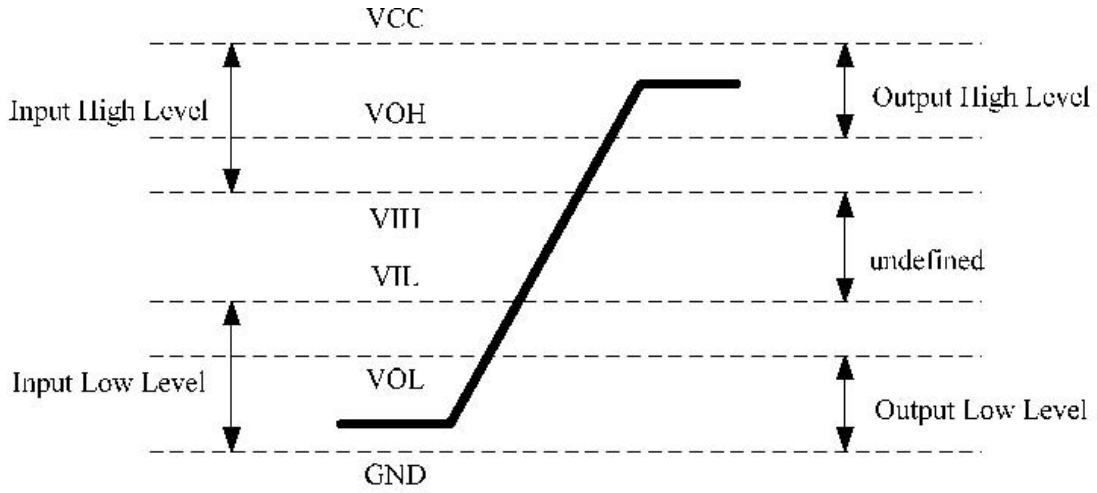


Figure 4: Interface I/O Voltage Diagram

4.2. *AC Characteristics*

4.2.1. Attribute Memory Read Timing

Table 12: Attribute Memory Read Timing

Speed Version	Symbol	300 ns	
Item		**Min ns.**	**Max ns.**
Read Cycle Time	tc (R)	300	
Address Access Time	ta (A)		300
Card Enable Access Time	ta (CE)		300
Output Enable Access Time	ta (OE)		150
Output Disable Time from CE	tdis (CE)		100
Output Disable Time from OE	tdis (OE)		100
Address Setup Time	tsu (A)	30	
Output Enable Time from CE	ten (CE)	5	
Output Enable Time from OE	ten (OE)	5	
Data Valid from Address Change	tv (A)	0	

Notes: All times are in nanoseconds. HD signifies data provided by the CompactFlash (CF) Card to the system. The CEx signal or both the HOE signal and the HWE signal shall be de-asserted between consecutive cycle operations.

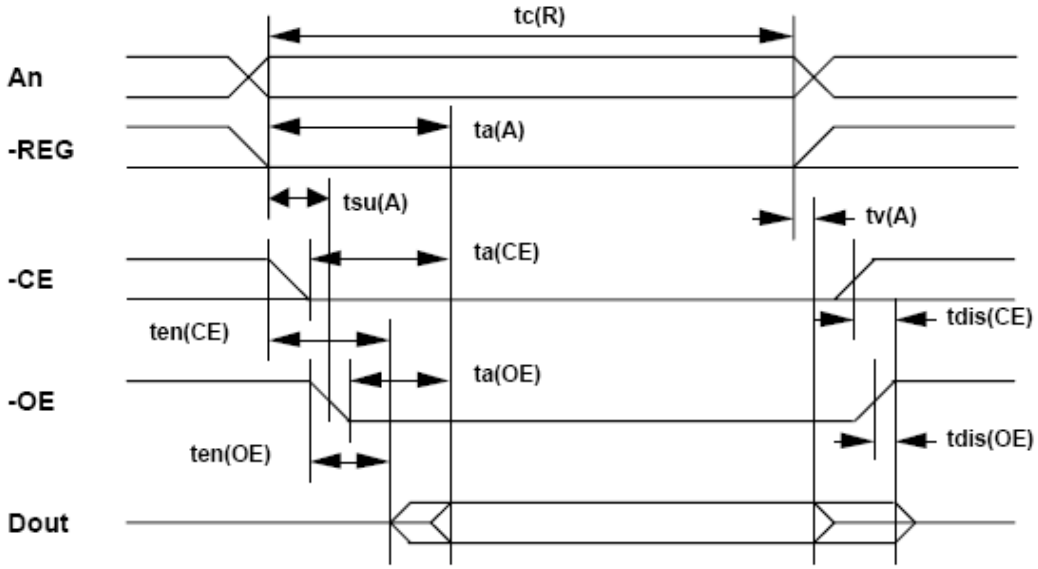


Figure 5: Attribute Memory Read Timing Diagram

4.2.2. Configuration Register (Attribute Memory) Write Time

Table 13: Configuration Register (Attribute Memory) Write Time

Speed Version	Symbol	250 ns	
Item		Min ns.	Max ns.
Write Cycle Time	tc (W)	250	
Write Pulse Width	tw (WE)	150	
Address Setup Time	tsu (A)	30	
Write Recovery Time	trec (WE)	30	
Data Setup Time for HWE	tsu (D-WEH)	80	
Data Hold Time	th (D)	30	

Notes: All times are in nanoseconds. HD signifies data provided by the system to the CompactFlash (CF) Card.

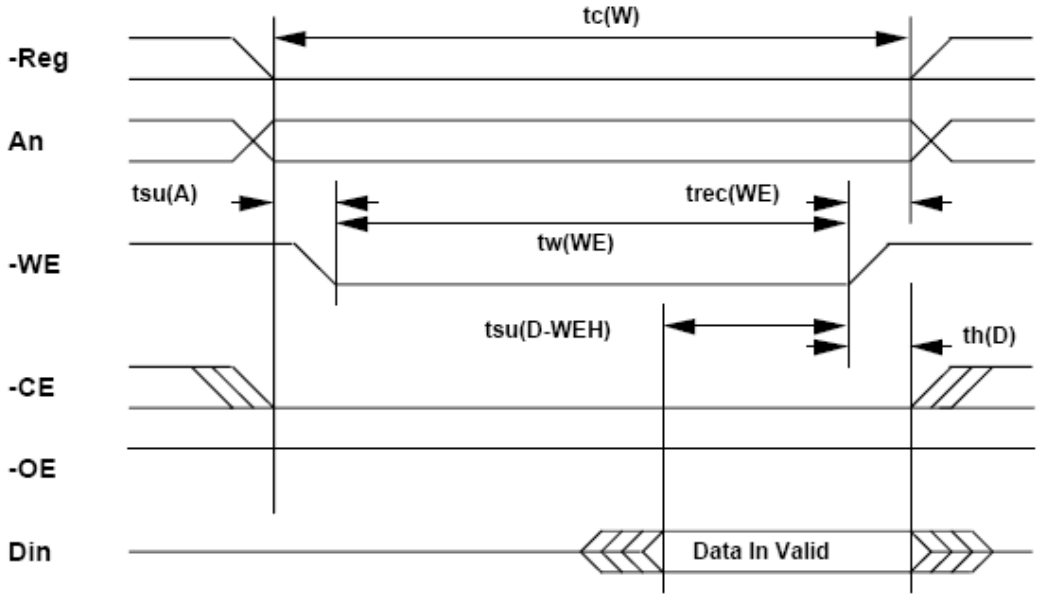


Figure 6: Configuration Register (Attribute Memory) Write Timing Diagram

4.2.3. Common Memory Read Timing

Table 14: Common Memory Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Output Enable Access Time	ta (OE)		125		60		50		40
Output Disable Time from	tdis (OE)		100		60		50		40
Address Setup Time	tsu (A)	30		15		10		10	
Address Hold Time	th (A)	20		15		15		10	
CE Setup before OE	tsu (CE)	0		0		0		0	
CE Hold following OE	th (CE)	20		15		15		10	
Wait Delay Falling from OE	tv (WT-OE)		35		35		35		Na[1]
Data Setup for Wait Release	tv (WT)		0		0		0		Na[1]
Wait Width Time [2]	tw (WT)		350		350		350		Na[1]

Notes:

1) IORDY is not supported in this mode

2) The Maximum load on IORDY is 1 LSTTL with 50pF (40pF below 120 nsec Cycle Time) total load. All times are in nanoseconds. HD signifies data provided by the CompactFlash (CF) Card to the system. The IORDYsignal may be ignored if the HOE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure.

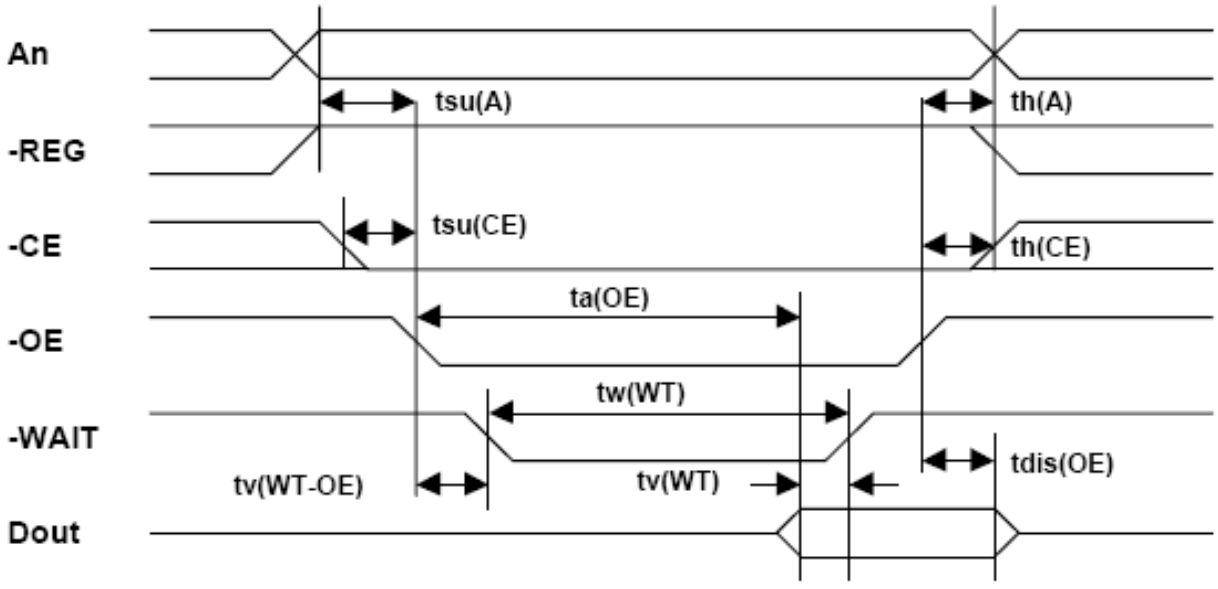


Figure 7: Common Memory Read Timing Diagram

4.2.4. Common Memory Write Timing

Table 15: Common Memory Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before WE	tsu (D-WEH)	80		50		40		30	
Data Hold following WE	th (D)	30		15		10		10	
WE Pulse Width	tw (WE)	150		70		60		55	
Address Setup Time	tsu (A)	30		15		10		10	
CE Setup before OE	tsu (CE)	0		0		0		0	
Write Recovery Time	trec (WE)	30		15		15		15	
Address Hold Time	th (A)	20		15		15		15	
CE Hold following OE	th (CE)	20		15		15		10	
Wait Delay Falling from OE	tv (WT-OE)		35		35		35		Na[1]
WE High from Wait Release	tv (WT)		0		0		0		Na[1]
Wait Width Time [2]	tw (WT)		350		350		350		Na[1]

Notes:

1) IORDY is not supported in this mode

2) The Maximum load on IORDY is 1 LSTTL with 50pF (40pF below 120 nsec Cycle Time) total load. All times are in nanoseconds. HD signifies data provided by the CompactFlash (CF) Card to the system. The IORDYsignal may be ignored if the HOE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure.

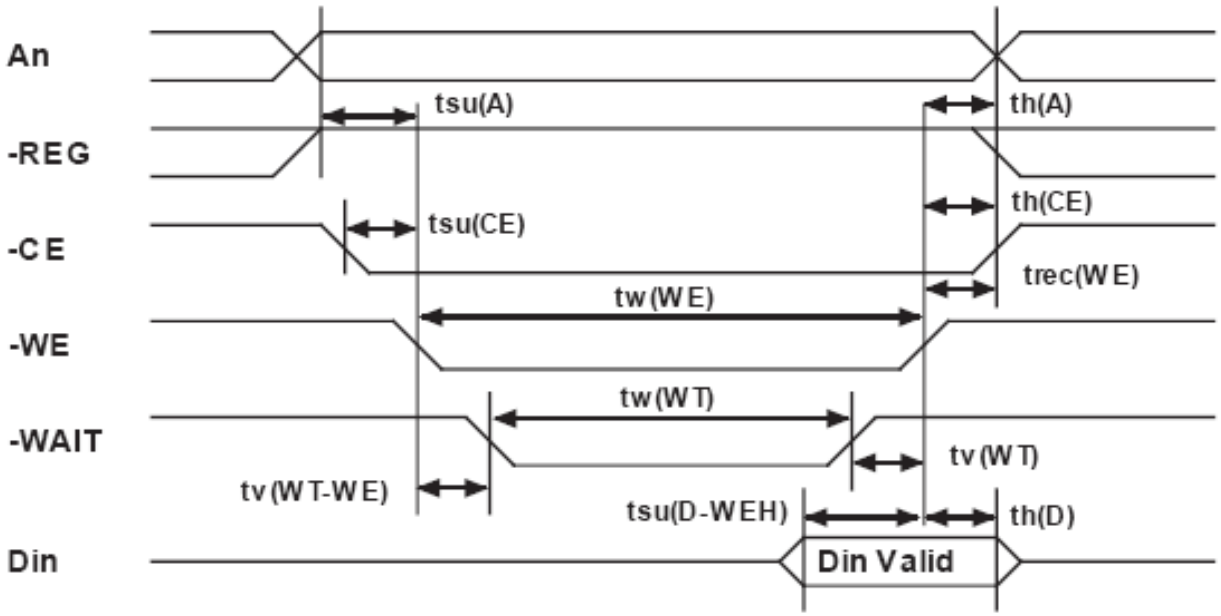


Figure 8: Common Memory Read Timing Diagram

4.2.5. I/O Read Timing

Table 16: I/O Read Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**	**Min ns.**	**Max ns.**
Data Delay after IORD	td (IORD)		100		50		50		45
Data Hold following IORD	th (IORD)	0		5		5		5	
IORD Width Time	tw (IORD)	165		70		65		55	
Address Setup before IORD	tsuHA (IORD)	70		25		25		15	
Address Hold following IORD	thA (IORD)	20		10		10		10	
CE Setup before IORD	tsuCE (IORD)	5		5		5		5	
CE Hold following IORD	thCE (IORD)	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	5		5		5		5	
REG Hold following IORD	thREG (IORD)	0		0		0		0	
INPACK Delay Falling from IORD	tdFINPACK (IORD)	0	45	0	Na[1]	0	Na[1]	0	Na[1]
INPACK Delay Rising from IROD	tdrINPACK(IORD)		45		Na[1]		Na[1]		Na[1]
IOIS16 Delay Falling From Address	tdfIOIS16(ADR)		35		Na[1]		Na[1]		Na[1]
IOIS16 Delay Rising From Address	tdrIOIS16(ADR)		35		Na[1]		Na[1]		Na[1]
Wait Delay Falling From IORD	tdWT(IORD)		35		35		35		Na[2]
Data Delay from Wait Rising	td(WT)		0		0		0		Na[2]
Wait Width Time [2]	tw(WT)		350		350		350		Na[2]

Notes:1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.

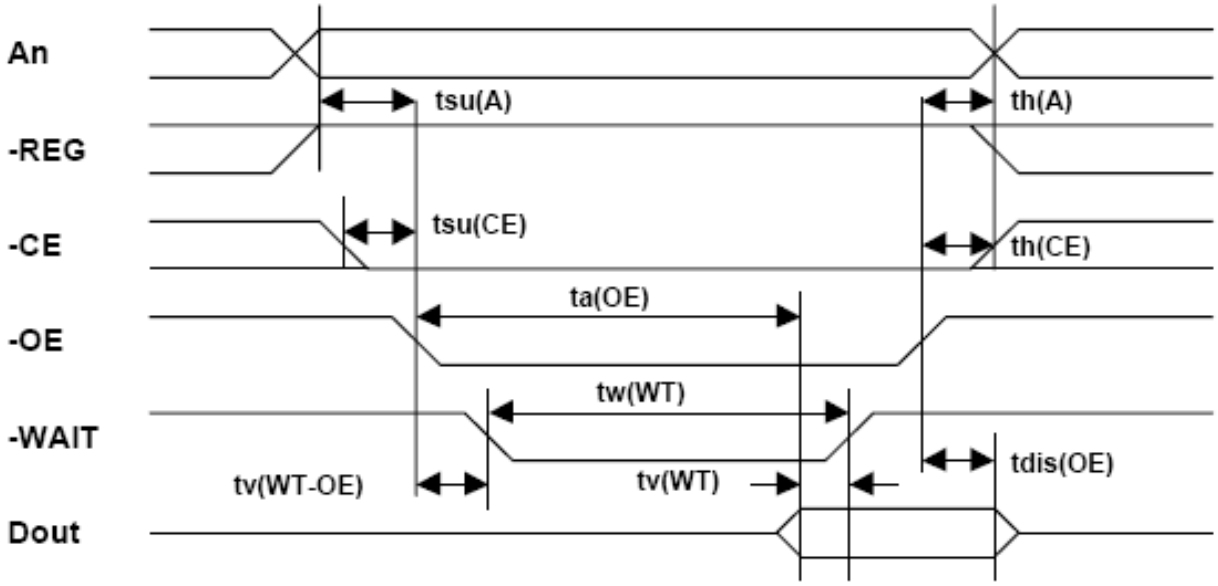


Figure 9: I/O Read Timing Diagram

4.2.6. I/O Write Timing

Table 17: I/O Write Timing

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before IOWR	tsu (IOWR)	60		20		20		15	
Data Hold following IOWR	th (IOWR)	30		10		5		5	
IOWR Width Time	tw (IOWR)	165		70		65		55	
Address Setup before IOWR	tsuA (IOWR)	70		25		25		15	
Address Hold following IOWR	thA (IOWR)	20		20		10		10	
CE Setup before IOWR	tsuCE (IOWR)	5		5		5		5	
CE Hold following IOWR	thCE (IOWR)	20		20		10		10	
REG Setup before IOWR	tsuREG(IOWR)	5		5		5		5	
REG Hold following IOWR	thREG (IOWR)	0		0		0		0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)		35		Na[1]		Na[1]		Na[1]
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)		35		Na[1]		Na[2]		Na[2]
Wait Delay Falling from IOWR	tdWT(IOWR)		35		35		Na[2]		Na[2]
IOWR High from Wait High [2]	tdrIOWR(WT)	0		0		0			Na[2]
Wait Width Time [2]	tw(IORDY)		350		350		350		Na[1]

Notes: 1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data

provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.

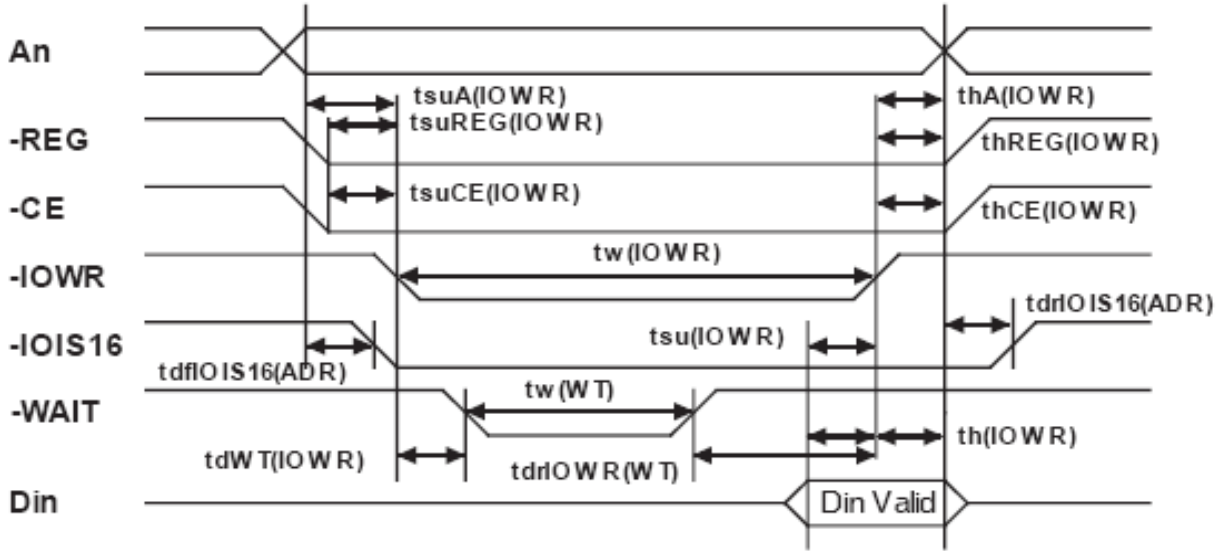


Figure 10: I/O Write Timing Diagram

4.2.7. True IDE PIO Mode Read/Write Timing

Table 18: True IDE PIO Mode Read/Write Timing

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t0	Cycle time (min)1	600	383	240	180	120
t1	Address Valid to HIOR/HIOW setup (min)	70	50	30	30	25
t2	HIOR/HIOW (min)1	165	125	100	80	70
t2	HIOR/HIOW (min) Register (8 bit)1	290	290	290	80	70
t2i	HIOR/HIOW recovery time (min)1	-	-	-	70	25
t3	HIOW data setup (min)	60	45	30	30	20
t4	HIOW data hold (min)	30	20	15	10	10
t5	HIOR data setup (min)	50	35	20	20	20
t6	HIOR data hold (min)	5	5	5	5	5
t6Z	HIOR data tristate (max)2	30	30	30	30	30
t7	Address valid to IOCS16 assertion (max)4	90	50	40	n/a	n/a
t8	Address valid to IOCS16 released (max)4	60	45	30	n/a	n/a
t9	HIOR/HIOW to address valid hold	20	15	10	10	10
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0
tA	IORDY Setup time3	35	35	35	35	35
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250
tC	IORDY assertion to release (max)	5	5	5	5	5

Notes:

(1) All timings are in nanoseconds. The maximum load on IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from IORDY high to HIOE high is 0 nsec, but minimum HIOE width shall still be met. (1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data.

(2) This parameter specifies the time from the negation edge of HIOE to the time that the data bus is no longer driven by the device. (3)The delay from the activation of HIOE or HIOW until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at tA after the activation of HIOE or HIOW, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of HIOE or HIOW, then tRD shall be met and t5 is not applicable. (4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid. (5) IORDY is not supported in this mode.

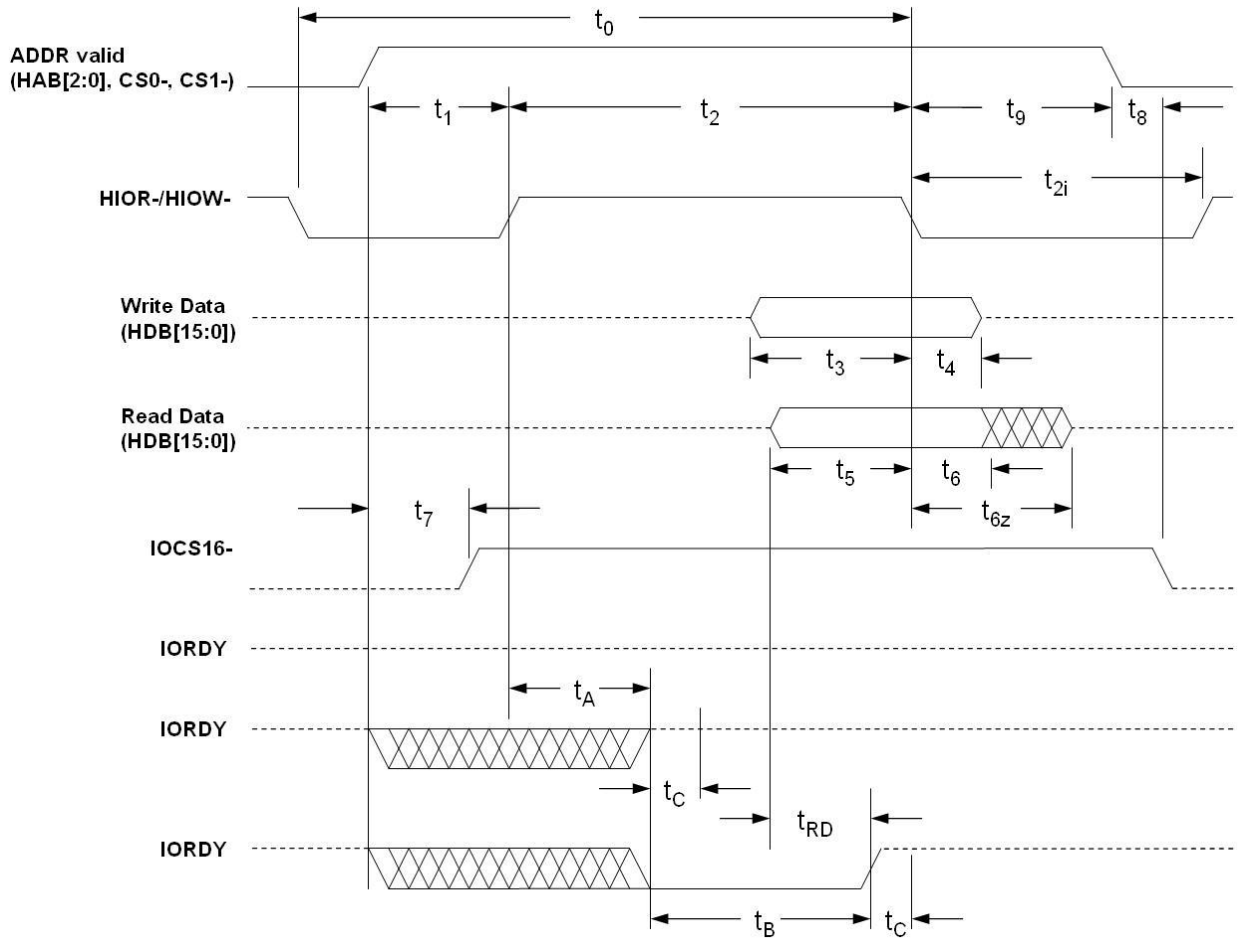


Figure 11: True IDE PIO Mode Read/Write Timing Diagram

Notes:

1) *Device address consists of CE0, CE1, and HA [2:0]*
2) *Data consist of HD [15:00] (16-bit) or HD [7:0] (8-bit)*
3) *IOCS16 is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.*
4) *The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of HIOE or HIOW. The assertion and negation of IORDY is described in the following three cases:*
   - *4-1) Device never negates IORDY: No wait is generated.*
   - *4-2) Device drives IORDY low before tA: wait generated. The cycle complete after IORDY is reasserted. For cycles where a wait is generated and HIOE is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.*

4.2.8. True IDE Multiword DMA Mode Read/Write Timing

Table 19: True IDE Multiword DMA Mode Read/Write Timing

Item		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
t_0	Cycle time (min)	480	150	120	100	80	1
t_D	HIOR / HIOW asserted width (min)	215	80	70	65	55	1
t_E	HIOR data access (max)	150	60	50	50	45	
t_F	HIOR data hold (min)	5	5	5	5	5	
t_G	HIOR/ HIOW data setup (min)	100	30	20	15	10	
t_H	HIOW data hold (min)	20	15	10	5	5	
t_I	DMACK(HREG) to HIOR/HIOW setup (min)	0	0	0	0	0	
t_J	HIOR / HIOW to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	HIOR negated width (min)	50	50	25	25	20	1
t_{KW}	HIOW negated width (min)	215	50	25	25	20	1
t_{LR}	HIOR to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	HIOW to DMARQ delay (max)	40	40	35	35	35	
t_M	CS1 CS0 valid to HIOR / HIOW	50	30	25	10	5	
t_N	CS1 CS0 hold	15	10	10	10	10	
t_Z	DMACK-	20	25	25	25	25	

Notes: t0 is the minimum total cycle time and tD is the minimum command active time, while tKR and tKW are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tKR, and tKW shall be met. The minimum total cycle time requirement is greater than the sum of tD and tKR or tKW for input and output cycles respectively. This means a host implementation can lengthen either or both of tD and either of tKR, and tKW as needed to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A device implementation shall support any legal host implementation.

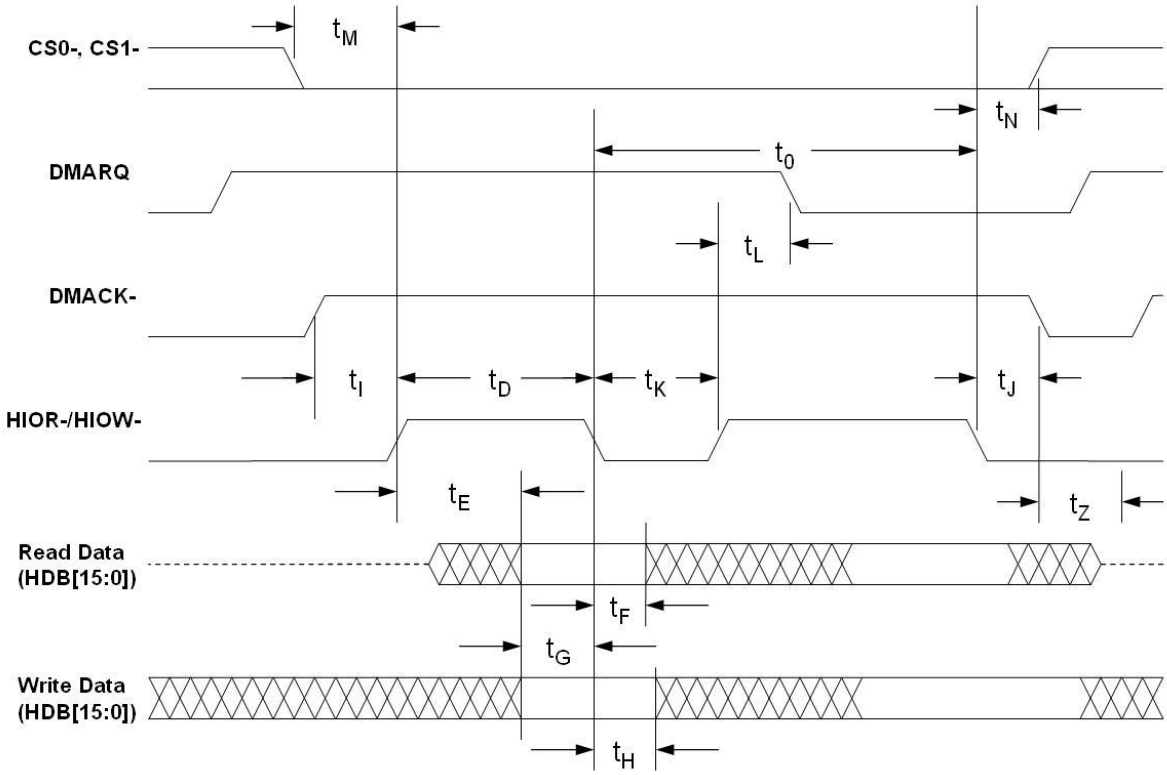


Figure 12: True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:

1) *If the CompactFlash (CF) Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.*
2) *This signal may be negated by the host to suspend the DMA transfer in progress.*

4.2.9. Ultra DMA Signal in Each Interface Mode

Table 20: Ultra DMA Signal in True IDE Mode

Signal	Type	(Non UDMA Memory Mode)	PC Card Memory Mode UDMA	PC Card IO Mode UDMA	TRUE IDE MODE UDMA
DMARQ	Output	(-INPACK)	-DMARQ	-DMARQ	DMARQ
HREG	Input	(-REG)	- DMARQ	DMARQ	- DMARQ
HIOW	Input	(-IOWR)	STOP[1]	STOP[1]	STOP[1]
HIOE	Input	(-IORD)	-HDMARDY(R) [1,2] HSTROBE(W) [1,3,4]	-HDMARDY(R) [1,2] HSTROBE(W) [1,3,4]	-HDMARDY(R) [1,2] HSTROBE(W) [1,3,4]
IORDY	Output	(-WAIT)	-DDMARDY(W) [1,3] DSTROBE(R) [1,2,4]	-DDMARDY(W) [1,3] DSTROBE(R) [1,2,4]	-DDMARDY(W) [1,3] DSTROBE(R) [1,2,4]
HD〔15:00〕	Bidir	(D〔15:00〕)	D〔15:00〕	D〔15:00〕	D〔15:00〕
HA〔10:00〕	Input	(A〔10:00〕)	A〔10:00〕[5]	A〔10:00〕[5]	A〔02:00〕[5]
CSEL	Input	(-CSEL)	-CSEL	-CSEL	-CSEL
HIRQ	Output	(READY)	READY	-INTRQ	INTRQ
CE1 CE2	Input	(-CE1) (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Notes:

1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.

2) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Read command.

3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.

4) The HSTROBE signals are active on both the rising and the falling edge.

5) Address lines 03 through 10 are not used in True IDE mode.

4.2.10. Ultra DMA Data Burst Timing Requirement

Table 21: Ultra DMA Data Burst Timing Requirement

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		Measure Location2 (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t2CYCTYP	240		160		120		90		60		Sender
tCYC	112		73		54		39		25		Note3
t2CYC	230		153		115		86		57		Sender
tDS	15.0		10.0		7.0		7.0		5.0		Recipient
tDH	5.0		5.0		5.0		5.0		5.0		Recipient
tDVS	70.0		48.0		31.0		20.0		6.7		Sender
tDVH	6.2		6.2		6.2		6.2		6.2		Sender
tCS	15.0		10.0		7.0		7.0		5.0		Device
tCH	5.0		5.0		5.0		5.0		5.0		Device
tCVS	70.0		48.0		31.0		20.0		6.7		Host
tCVH	6.2		6.2		6.2		6.2		6.2		Host
tZFS	0		0		0		0		0		Device
tDZFS	70.0		48.0		31.0		20.0		6.7		Sender
tFS		230		200		170		130		120	Device
tLI	0	150	0	150	0	150	0	100	0	100	Note4
tMLI	20		20		20		20		20		Host
tUI	0		0		0		0		0		Host
tAZ		10		10		10		10		10	Note5
tZAH	20		20		20		20		20		Host
tZAD	0		0		0		0		0		Device
tENV	20	70	20	70	20	70	20	55	20	55	Host
tRFS		75		70		60		60		60	Sender
tRP	160		125		100		100		100		Recipient
tIORDYZ		20		20		20		20		20	Device
tZIORDY	0		0		0		0		0		Device
tACK	20		20		20		20		20		Host
tSS	50		50		50		50		50		Sender

Notes: All Timings in ns

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector.

3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender.

4) The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5) The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

6) See the AC Timing requirements in 4.2.12.Ultra DMA AC Signal Requirements.

4.2.11. Ultra DMA Data Burst Timing Descriptions

Table 22: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
T2CYCTYP	Typical sustained average two cycle time	
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge next falling edge of STROBE)	
tDS	Data setup time at recipient (from data valid until STROBE edge)	2,5
tDH	Data hold time at recipient (from STROBE edge until data may become invalid)	2,5
tDVS	Data valid setup time at sender (from data valid until STROBE edge)	3
tDVH	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
tCS	CRC word setup time at device	2
tCH	CRC word hold time device	2
tCVS	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
tCVH	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.	
tDZFS	Time from data output released-to-driving until the first transition of critical timing.	
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
tLI	Limited interlock time	1
tMLI	Interlock time with minimum	1
tUI	Unlimited interlock time	1
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)	
tZAH	Minimum delay time required for output	
tZAD	drivers to assert or negate (from released)	
tENV	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
tRP	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
tIORDYZ	Maximum time before releasing IORDY	
tZIORDY	Minimum time before driving IORDY	4
tACK	Setup and hold times for -DMACK (before assertion or negation)	
tSS	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

(1) The parameters tUI, tMLI (in Figure16: Ultra DMA Data-In Burst Device Termination Timing and Figure 17: Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum.

(2) 80-conductor cablingshall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2.

(3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

(4) For all timing modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

(5) The parameters tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

4.2.12. Ultra DMA Sender and Recipient IC Timing Requirements

Table 23: Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tDSIC	14.7		9.7		6.8		6.8		4.8	
tDHIC	4.8		4.8		4.8		4.8		4.8	
tDVSIC	72.9		50.9		33.9		22.6		9.5	
tDVHIC	9.0		9.0		9.0		9.0		9.0	
tDSIC	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)									
tDHIC	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)									
tDVSIC	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)									
tDVHIC	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)									

Notes:

(1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

(2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).

(3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

4.2.13. Ultra DMA AC Signal Requirements

Table 24: Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
SRISE	Rising Edge Slew Rate for any signal		1.25	1
SFALL	Falling Edge Slew Rate for any signal		1.25	1

Notes:

(1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector. The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

4.2.14. Ultra DMA Data-In Burst Initiation Timing

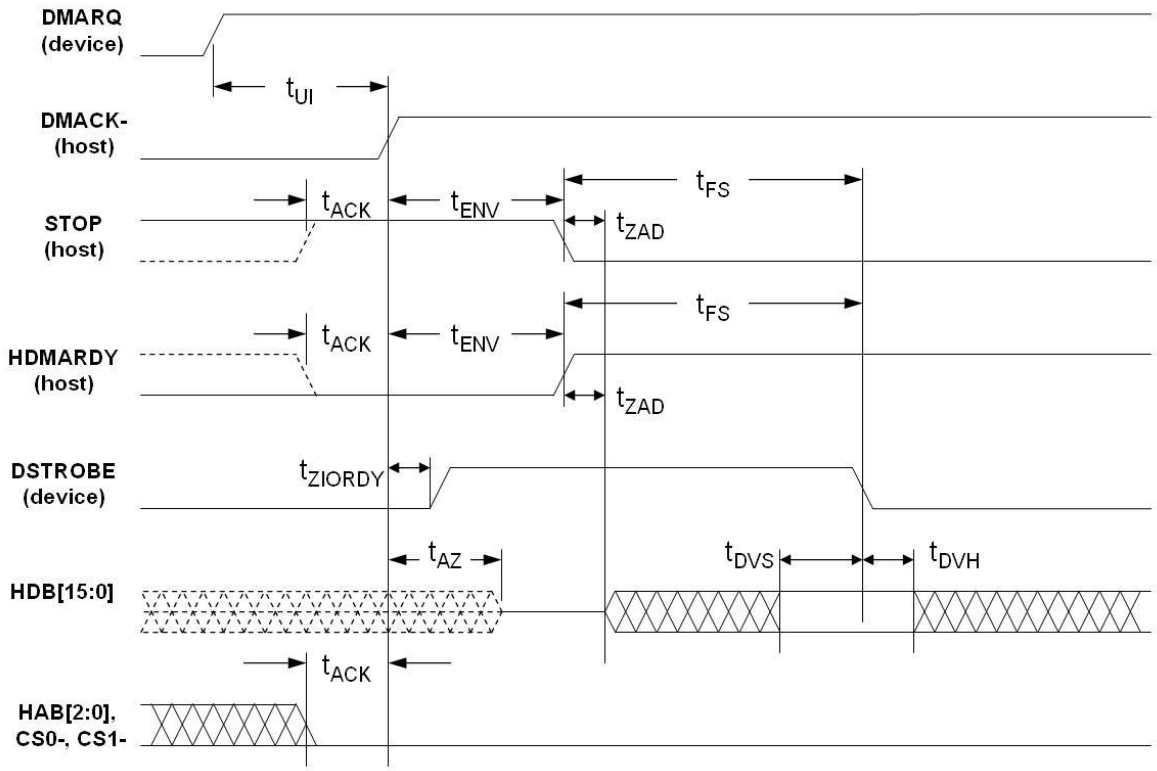


Figure 13: Ultra DMA Data-in Burst Initiation Timing Diagram

Note:

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH.

NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the IORDY:-DDMARDY: DSTROBE,-IORD:-HDMARDY: HSTROBE, and –IOWR:STOP signal lines are not in effect until DMARQ and –DMACK are asserted.

HAB〔02:00〕,-CS0 & -CS1 are True IDE mode signal definitions.

4.2.15. Sustained Ultra DMA Data-In Burst Timing

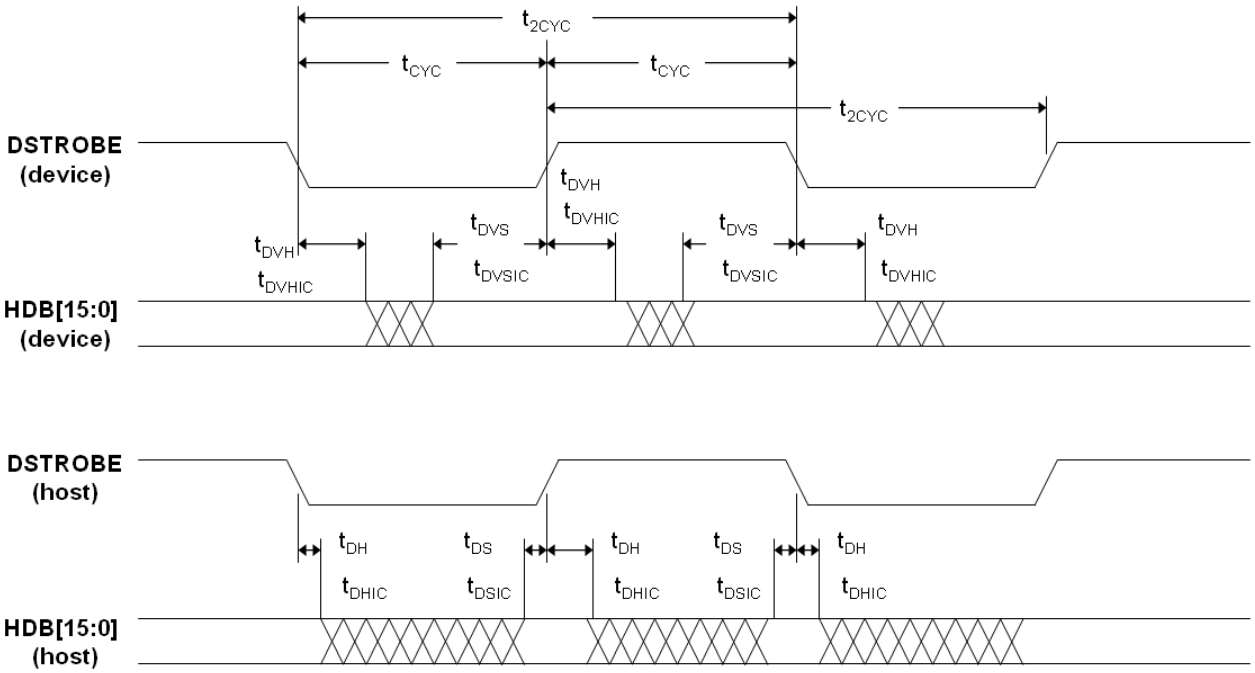


Figure 14: Sustained Ultra DMA Data-in Burst Initiation Timing Diagram

Note:

HDB [15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

4.2.16. Ultra DMA Data-In Burst Host Pause Timing

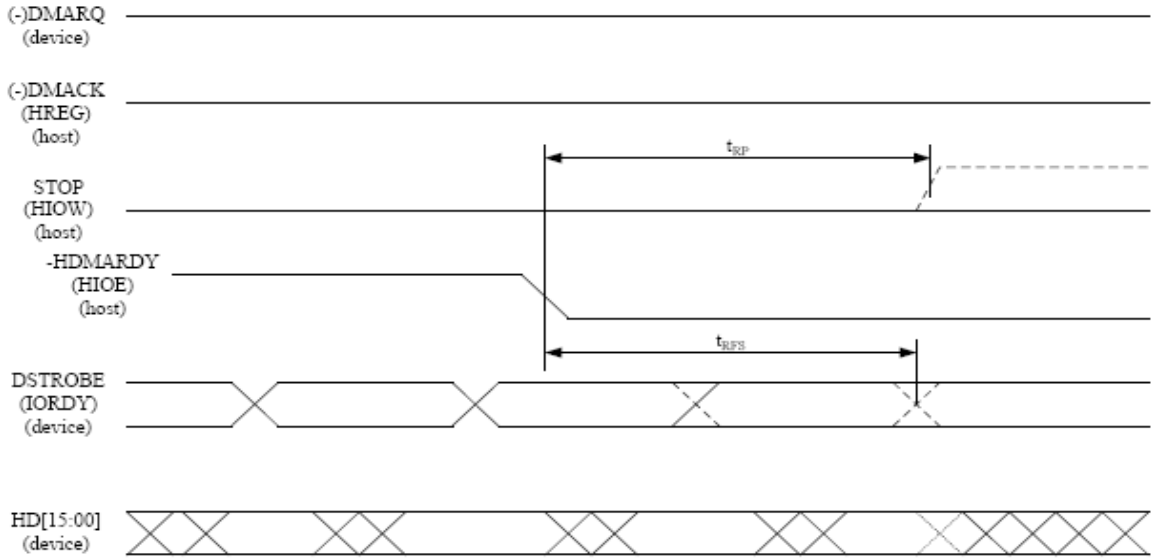


Figure 15: Ultra DMA Data-In Burst Host Pause Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

(1) The host may assert STOP to request termination of the Ultra DMA data burst no sooner than tRP after –HDMARY is negated.

(2) After negating –HDMARDY, the host may receive zero, one, two, or three more data words from the device.

(3) The bus polarity of the (-) DMARQ and (-) DMACK signals is dependent on the active interface mode.

4.2.17. Ultra DMA Data-In Burst Device Termination Timing

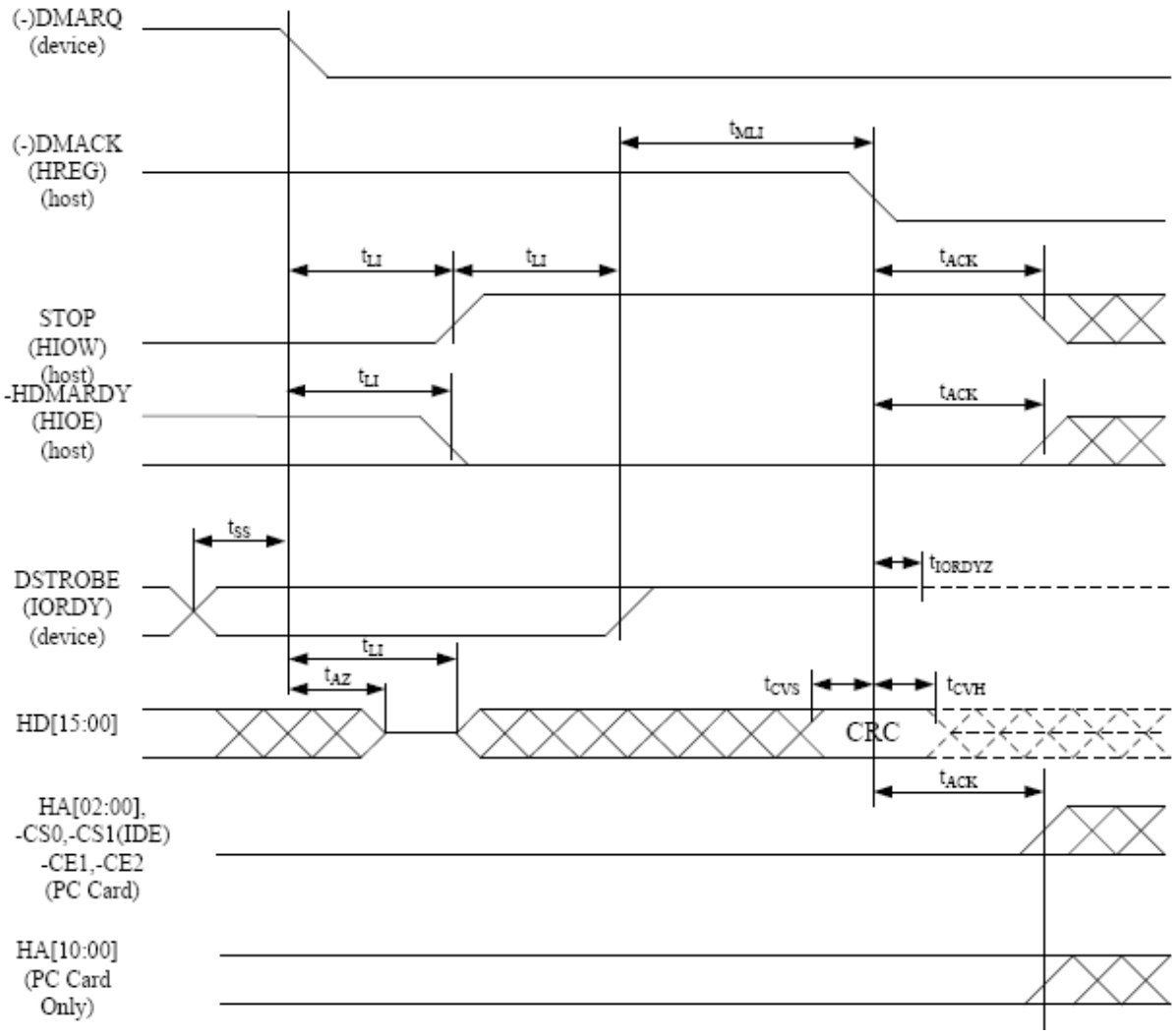


Figure 16: Ultra DMA Data-In Burst Device Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0& -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.18. Ultra DMA Data-In Burst Host Termination Timing

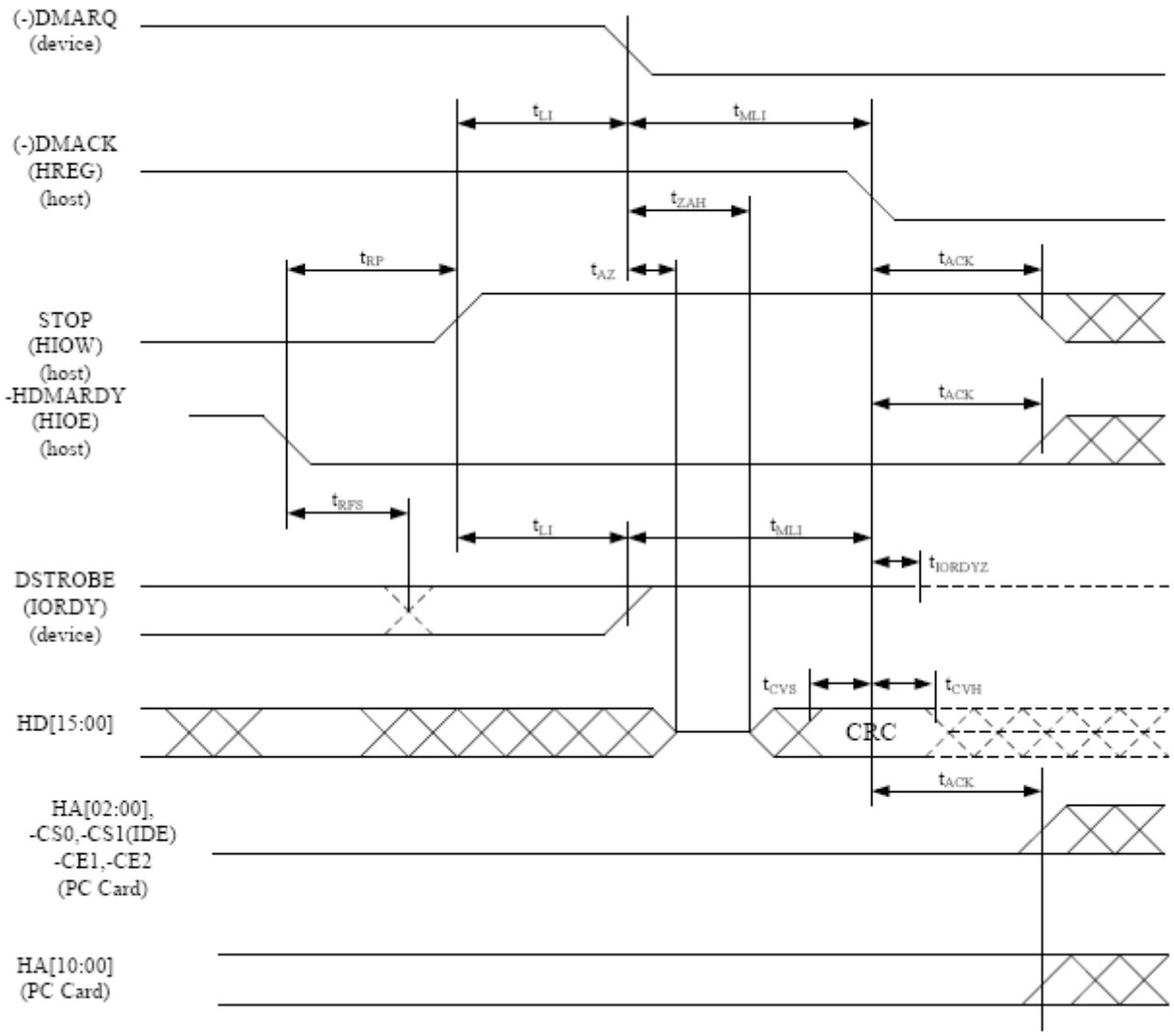


Figure 17: Ultra DMA Data-In Burst Host Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0& -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and –CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.19. Ultra DMA Data-Out Burst Host Initiation Timing

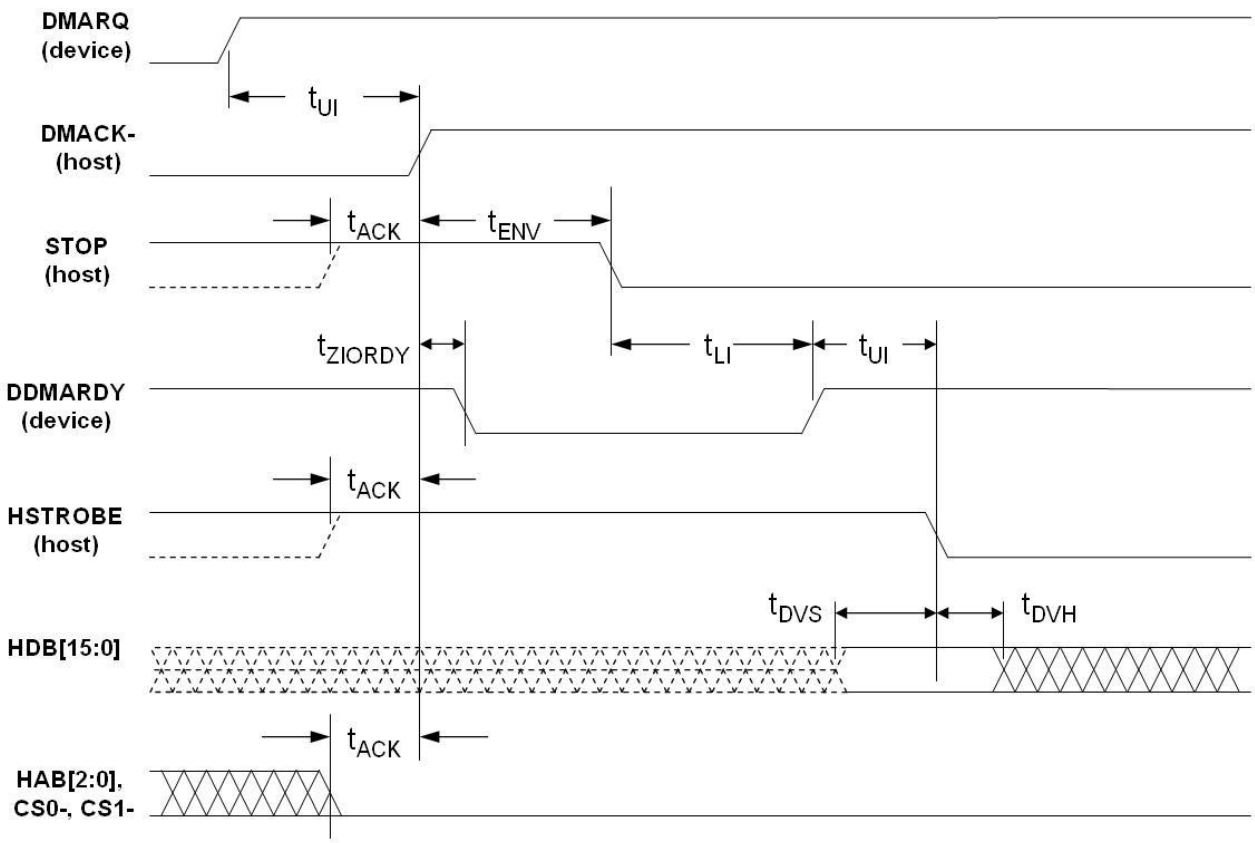


Figure 18: Ultra DMA Data-Out Burst Initiation Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, DDMARD, and HSTROBE signal lines are no in effect after DMARQ and DMACK are asserted. HAB[02:00], -CS0& -CS1 are True IDE mode signal definitions.

4.2.20. Sustained Ultra DMA Data-Out Burst Host Initiation Timing

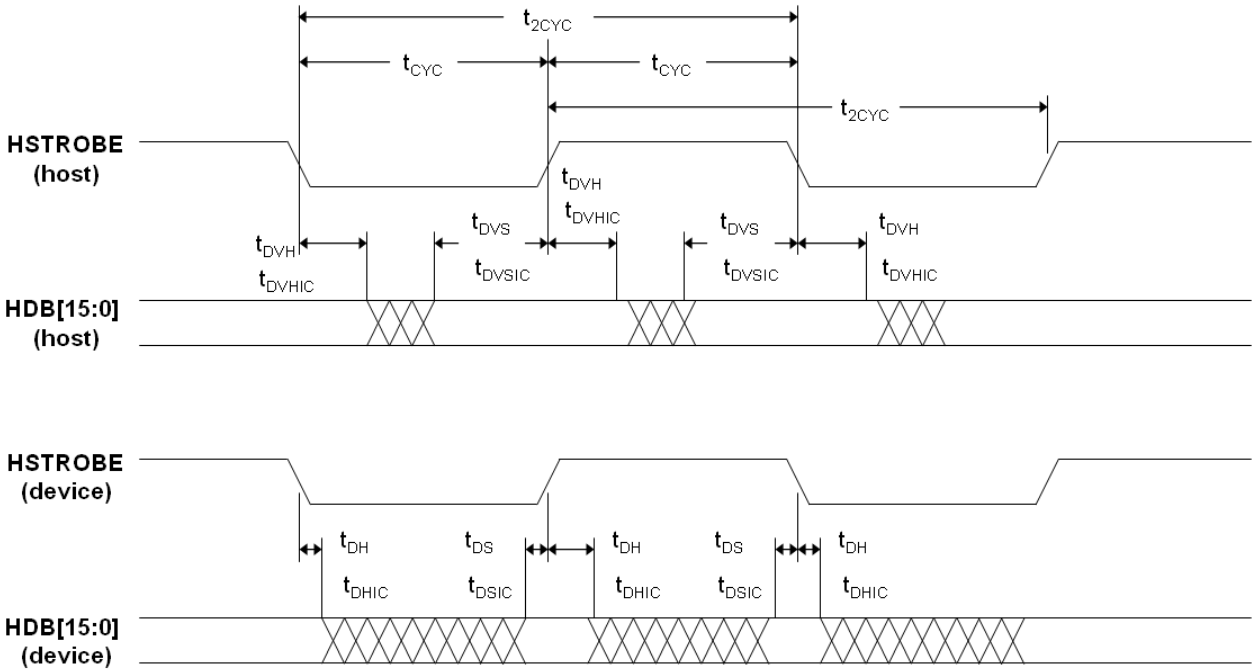


Figure 19: Sustained Ultra DMA Data-Out Burst Timing Diagram

Notes: Data (HDB[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable Setting time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

4.2.21. Ultra DMA Data-Out Burst Device Pause Timing

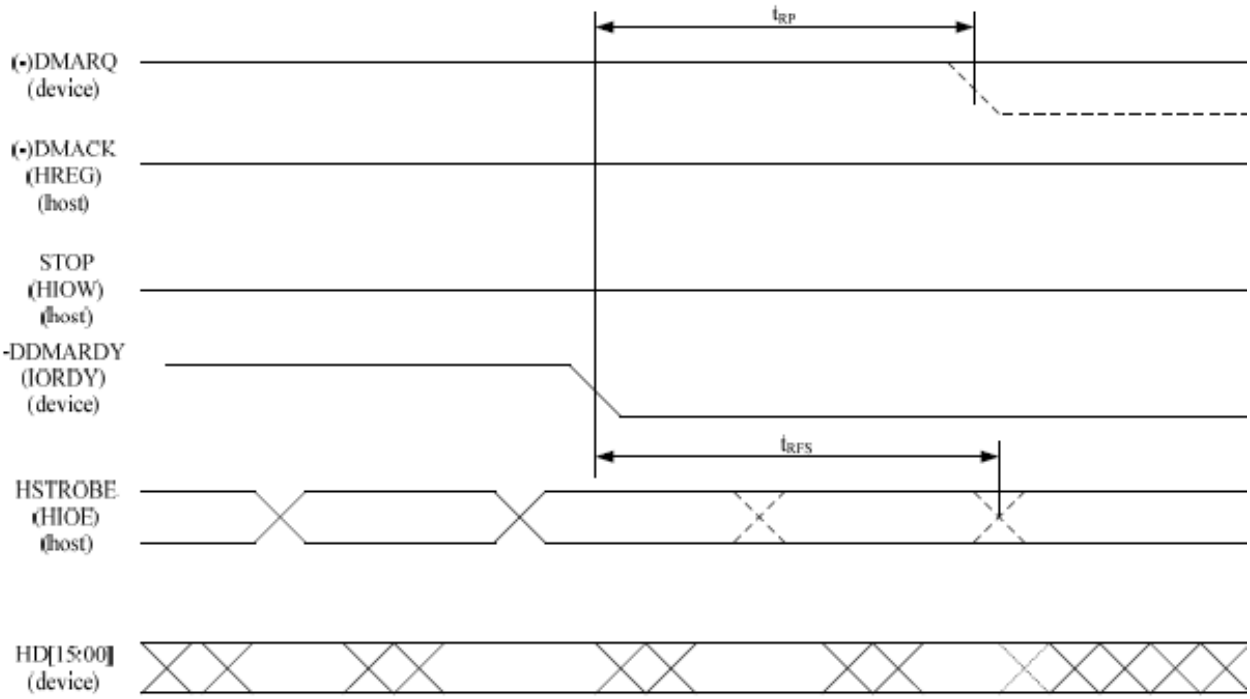


Figure 20: Ultra DMA Data-out Burst Device Pause Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: (1) The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than tRP after –DDMARDY, is negated.

(2) After negating –DDMARDY, the device may receive zero, one, two, or three more data words from the host.

(3) The bus polarity of DMARQ and DMACK depend on the active interface mode.

4.2.22. Ultra DMA Data-Out Burst Device Termination Timing

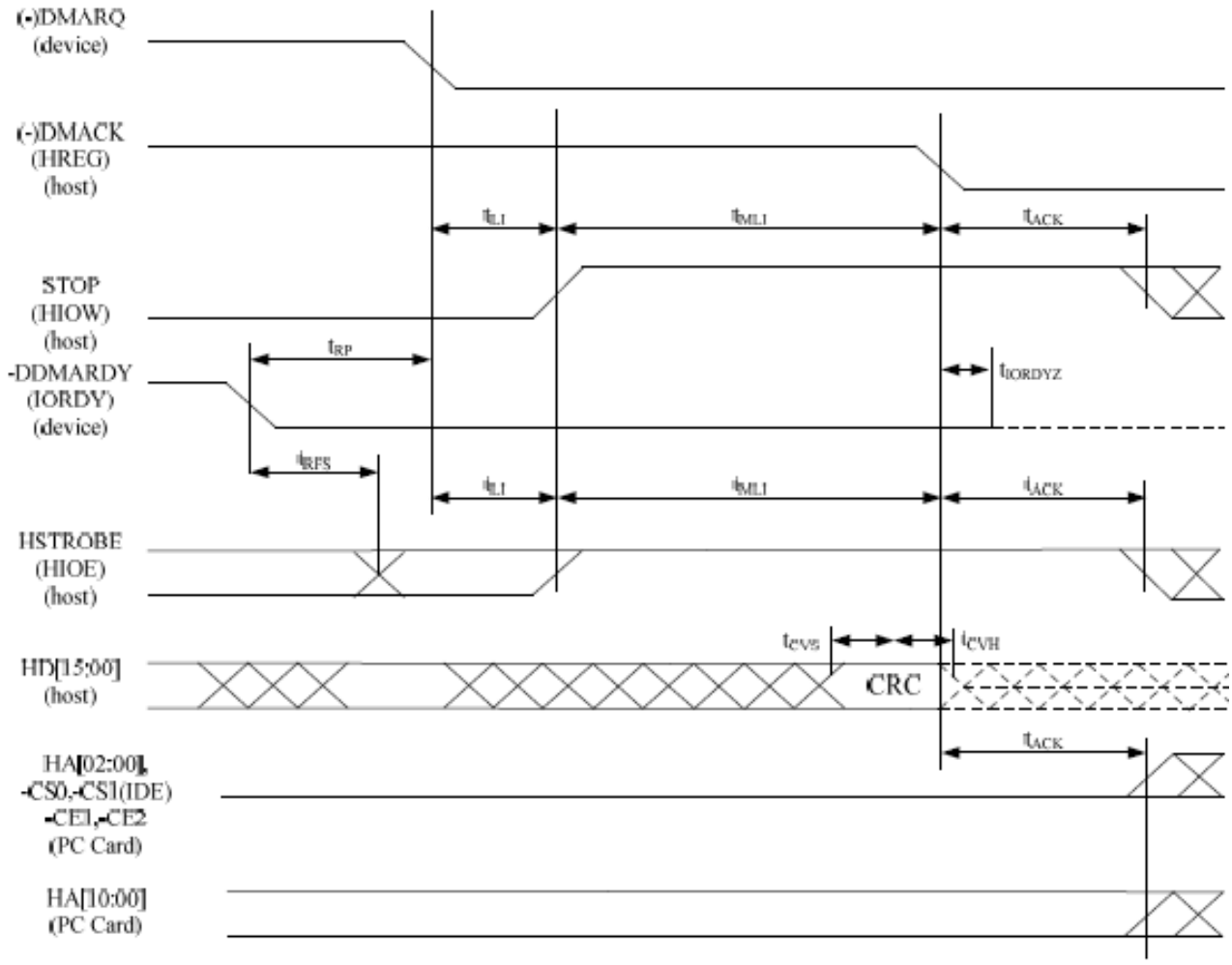


Figure 21: Ultra DMA Data-Out Burst Device Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[00:02], -CS0& -CS1 are True IDE mode signal definitions. HA[00:10], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

4.2.23. Ultra DMA Data-Out Burst Host Termination Timing

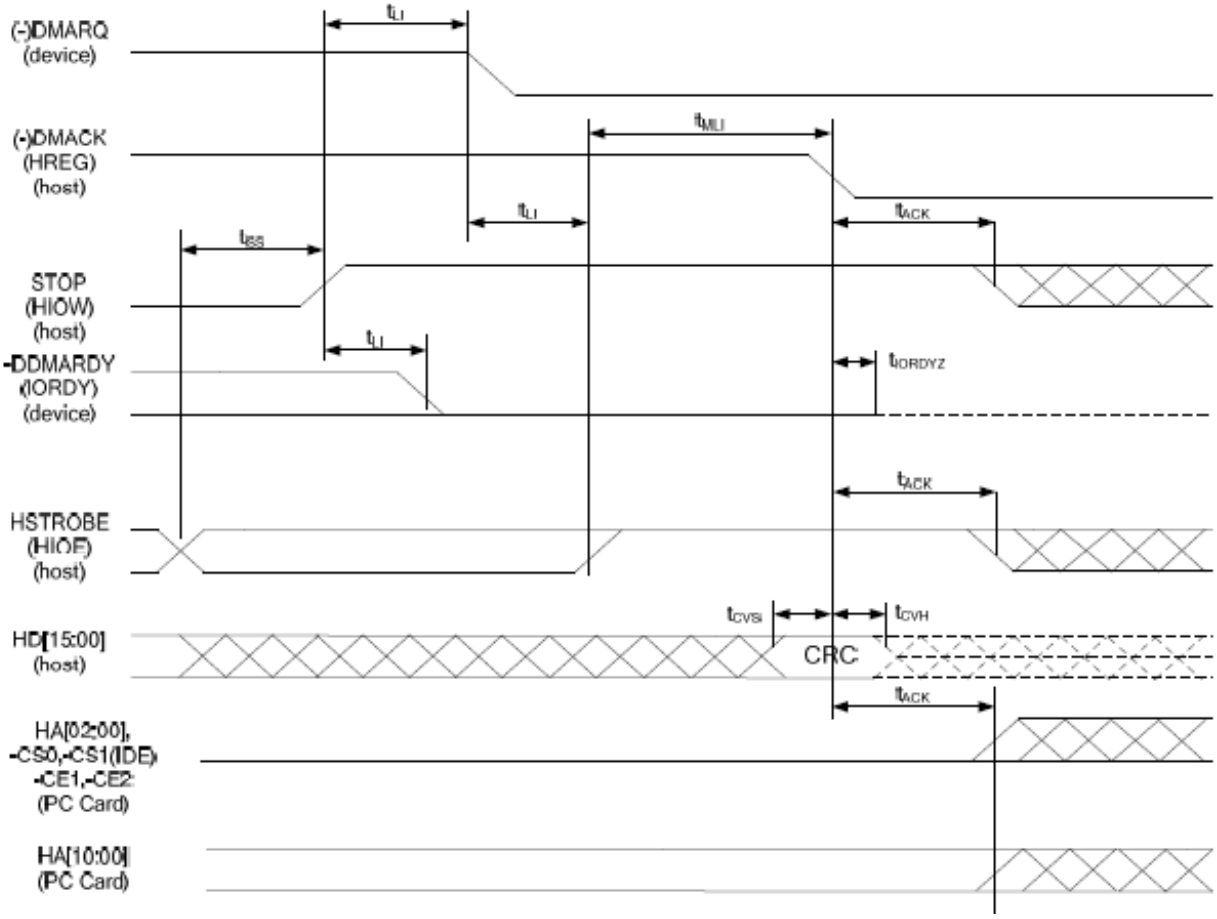


Figure 22: Ultra DMA Data-Out Burst Host Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0& -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

5. Interface Register Definition

5.1. *Device Address*

This controller receives commands from the host only when it is the selected device by checking the DEV bit in the Device Register.

This interface is for the host to program and perform commands and return status.

Table 25: Device Address Commands

CS1–	CS0–	A2	A1	A0	DMACK–	DIOR– = L	DIOW– = L
1	0	0	0	0	1	Data register	Data register
1	1	X	X	X	0	DMA Data RD	DMA Data Write
1	0	0	0	1	1	Error register	Feature register
1	0	0	1	0	1	Sector Count register	Sector Count register
1	0	0	1	1	1	LBA Low register	LBA Low register
1	0	1	0	0	1	LBA Mid register	LBA Mid register
1	0	1	0	1	1	LBA High register	LBA High register
1	0	1	1	0	1	Device register	Device register
1	0	1	1	1	1	Status register	Command register
0	1	1	1	0	1	Alt. Status register	Device Control register

5.2. *I/O Register Descriptions*

The Command Block registers are used for the host to send commands to this controller or for this controller to post status. These registers include the LBA High, LBA Mid, LBA Low, Device, Sector Count, Command, Status, Features, Error and Data Registers. The Control Block register is used for device control and to post alternate status. These registers include Device Control and Alternate Status registers.

For the detail field/bit description of every register, please refer to the ATAPI-5 specification.

(1) Alternate Status Register

This register contains the same information as the Status register in the Command Block.

(2) Command Register

This register contains the command code being sent. This controller begins immediately to execute the command after receipt of the command

(3) DMA Data Port

This port is only accessed for the host DMA data transfers when DMACK– and DMARQ are asserted. The data is 16-bits in width.

(4) Data Register

This register is accessed for the host PIO data transfer only when DRQ is set to one and DMACK– is not asserted. The contents of this register are not valid while it is in the Sleep mode. This register is 16 bits wide.

(5) Device Register

This register is for the host to set bit 4, DEV, of this register to selects the device. Other bis in this register are command dependent.

(6) Device Control Register

This register allows the host to software reset attached devices and to enable or disable the assertion of the INTRQ signal by a selected device. When this register is written, the controller will respond to the write no matter the device is selected or not. And this controller will respond to the SRST bit when in the SLEEP mode.

(7) Error Register

At command completion of any command, the contents of this register are valid when the ERR bit is set to one in the Status register.

(8) Feature Register

This register is writing only, If this address is reading by the host, the content read by the host will be the Error register. The content of this register is command dependent.

(9) LBA High Register

This register contains the high order bits of logic block address and becomes a command parameter when Command register is written.

(10) LBA Low Register

This register contains the low order bits of logic block address and becomes a command parameter when Command register is written.

(11) LBA Mid Register

This register contains bit 15-8 of logic block address and becomes a command parameter when Command register is written.

(12) Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation.

(13) Status Register

This register contains the device status. The contents of this register are updated to reflect the current state of the device.

6. Software Specification

6.1. ATA Command Set

The following table summarizes the commands supported by the controller.

Table 26: ATA Commands Supported

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98H or E5H	-	-	-	-	D	-
1	Execute Device Diagnostic	90H	-	-	-	-	D	-
1	Erase Sector(s)	C0H	-	Y	Y	Y	Y	Y
2	Format Track	50H	-	Y	-	Y	Y	Y
1	Identify Device	ECH	-	-	-	-	D	-
1	Idle	97H or E3H	-	Y	-	-	D	-
1	Idle immediate	95H or E1H	-	-	-	-	D	-
1	Initialize Device Parameters	91H	-	Y	-	-	Y	-
1	Read Buffer	E4H	-	-	-	-	D	-
1	Read DMA	C8H	-	Y	Y	Y	Y	Y
1	Read Long Sector	22H or 23H	-	-	Y	Y	Y	Y
1	Read Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH	-	-	-	-	D	-
1	Request Sense	03H	-	-	-	-	D	-
1	Seek	7XH	-	-	Y	Y	Y	Y
1	Set Features	EFH	Y	-	-	-	D	-
1	Set Sleep Mode	99H or E6H	-	-	-	-	D	-
1	SMART	B0H	-	-	-	-	D	-
1	Standby	96H or E2H	-	-	-	-	D	-
1	Standby Immediate	94H or E0H	-	-	-	-	D	-
2	Write Buffer	E8H	-	-	-	-	D	-
2	Write DMA	CAH	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
2	Write Sector(s) without Erase	38H	-	Y	Y	Y	Y	Y

Notes:

FR: Feature Register

SC: Sector Count Register

SN: Sector Number Register

CY: Cylinder Registers

DH: Card/Device/Head Register

LBA: LBA Block Address Mode Supported

Y: Y: The register contains a valid parameter for this command. For Card/Device/Head Register Y means both the CompactFlash Storage Card and head parameter are used; D –only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command description for use).

6.2. *ATA Command Description*

(1) Check Power Mode – 98H or E5H

This command checks the power mode: If the CompactFlash Storage is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the CompactFlash Storage Card is in idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

Register	7	6	5	4	3	2	1	0
Command(7)	98h or E5h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(2) Execute Device Diagnostic – 90H

Register	7	6	5	4	3	2	1	0
Command(7)	90h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card. When the diagnostic command is issued in a PCMCIA configuration mode, this command runs only on the CompactFlash Storage Card that is addressed by the Drive/Head register. This is because PCMCIA card interface does not allow for direct inter-drive communication (such as the ATA PDIAG and DASP signals). When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices. The Diagnostic codes are shown in Table 27. Diagnostic Codes are returned in the Error Register at the end of the command.

Table 27: Diagnostic

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controller Microprocessor Error
8Xh	Slave Error in True IDE Mode

(3) Erase Sector(s) – C0h

This command is used to pre-erase and condition data sectors in advance of a Write thout Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

Register	7	6	5	4	3	2	1	0
Command(7)	C0h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

(4) Format Track – 50H

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

Register	7	6	5	4	3	2	1	0
Command(7)	50h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	X (LBA 7-0)							
Sector Count(2)	Count(LBA mode only)							
Feature(1)	X							

(5) Identify Device – ECH

Register	7	6	5	4	3	2	1	0
Command(7)	ECh							
C/D/H(6)	X	X	X	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 28. All reserved bits or words are zero. Hosts should not depend in obsolete words in Identify Device containing 0. Table 28 specifies each filed in the data returned by the Identify Device Command. In Table 28, X indicates a numeric nibble vale specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 28: Identify Device Commands

Word	Description	Value
0	General Configuration Bit 15 0=ATA device Bit 14:8 Retired Bit 7:6 Obsolete Bit 5:3 Retired Bit 2 Response incomplete Bit 1 Retired Bit 0 reserved	045Ah
1	Number of logical cylinders	XXXXh
2	Specific configuration	0000h
3	Number of logical heads	0010h
4-5	Retired	0000h 0200h
6	Number of logical sectors per logical track	00XXh
7-8	Number of sectors per card	XXXXh
9	Retired	0000h
10-19	Serial number in 20 ASCII	Aaaa
20-21	Retired	0002h 0001h

22	Obsolete	0004h
23-26	Firmware revision in 8 ASCII	Aaaa
27-46	Model number in 40 ASCII	Aaaa
47	15-8: 80 7-0: 00h Reserved 01h-FFh: Maximum number of sectors that shall be transferred per DRQ data block on READ/WRITE Multiple commands	80 XXh
48	Trusted Computing feature set options 15 shall be cleared to zero 14 shall be set to one 13:1 Reserved for the Trusted Computing Group 0 0 = Trusted Computing feature set is not supported	0000h
49	Capabilities 15-14: Reserved for the IDENTIFY PACKET DEVICE command. 13: 1=Standby timer values as specified in this standard are supported 0:Standby timer values shall be managed by the device 12: Reserved for the IDENTIFY PACKET DEVICE command 11: 1=IORDY supported 0=IORDY may be disabled 10 1: IORDY may be disabled 9 1=LBA supported 8 1=DMA supported. 7-0 Retired	0F00h
50	Capabilities 15: Shell be cleared to zero 14: Shall be set to one 13: 2 Reserved 1 Obsolete 0 0	0000h
51	PIO data transfer cycle timing mode	0200h
52	Obsolete	0000h
53	15 Free-fall control Sensitivity 00h: Vendor‟s recommended setting 7:3 Reserved 2: 1=the fields reported in word 88 are valid 1: 1=the fields reported in words (70:64) are valid 0: Obsolete	0007h
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh

56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15:9 Reserved 8 0: Multiple sector setting is invalid 7:0 Current setting for number of logical sectors that shall be transferred per DRQ data block on READ/WRITE Multi commands	01XXh
60-61	Total number of user address sectors(DWord)	XXXXXXXXh
62	Obsolete	0000h
63	Multi-word DMA transfer(Not support)	0007h
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds In PCMCIA mode this value shall be 0h	0078h
66	Manufacturer‟s recommended Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds In PCMCIA mode this value shall be 0h	0078h
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds	0078h
69-74	Reserved	0000h
75	No DMA QUEUED command supports	0000h
76	Serial ATA Capabilities 15:11 Reserved for Serial ATA 10 1= Supports Phy Event Counters 9 1= Supports receipt of host initiated power management Requests 8 0= No Support native Command Queuing 7:3 Reserved for future SATA signaling speed grades 2 1=Supports SATA Gen2 Signaling Speed (3.0Gb/s) 1 1=Support SATA Gen1 Signaling Speed (1.5Gb/s) 0 Shall be cleared to zero	0000h
77	Reserved for Serial ATA	0000h

78	Serial ATA features supported 15:7 Reserved for Serial ATA 6 0=Device not supports Software Settings Preservation 5 Reserved for Serial ATA 4 0= Device not supports in-order data delivery 3 0= Device not supports initiating power management 2 0= Device not supports DMA Setup auto-activation 1 0= Device not supports non-zero buffer offsets 0 Shall be cleared to zero	0000h
79	Serial ATA feature enabled 15:7 Reserved for Serial ATA 6 0=Software Settings Preservation not enabled 5 0=Reserved for Serial ATA 4 0= In-order data delivery not enabled 3 0= Device initiated power management not enabled 2 0= DMA setup auto-activation not enabled 1 0= Non-zero buffer offsets not enabled 0 Shall be cleared to zero	0000h
80-81	ATA Version support (ATA5)	0020 0000h
82	Command and feature sets supported 15 0 = Obsolete 14 0 = NOP Command not supported 13 0 = READ BUFFER Command not supported 12 0 = WRITE BUFFER Command not supported 11 0 = Obsolete 10 0 = Host Protected Area Feature Set not supported 9 0 = DEVICE RESET Command not supported 8 0 = SERVICE Interrupt not supported 7 0 = RELEASE Interrupt not supported 6 1 = Look-ahead supported 5 1 = Write Cache supported 4 0 = indicate that the PACKET feature set is not supported 3 1 = mandatory Power Management Feature Set supported 2 0 = Obsolete 1 0 = Security Mode Feature Set not supported 0 1 = SMART Feature Set supported	7008h

83	Command and feature sets supported 15 Shall be cleared to zero 14 Shall be set to one 13 0 = FLUSH CACHE EXT Command not supported 12 1 = mandatory FLUSH CACHE Command supported 11 0 = Device Configuration Overlay feature set not supported 10 0 = 48-Bit Address feature set not supported 9 0 = Automatic Acoustic Management feature set not supported 8 0 = SET MAX security extension not supported 7 0 = See Address Offset Reserved Area Boot, INCITS TR27:2001	5004h
	6 0 = SET FEATURES subcommand not required to spin-up after power-up 5 0 = Power-Up in Standby feature set supported 4 0 = Removable Media Status Notification feature set not supported 3 0 = Advanced Power Management feature set not supported 2 0 = CFA feature set not supported 1 0 = READ/WRITE DMA QUEUED not supported 0 1 = DOWNLOAD MICROCODE Command supported	
84	Command Set/Feature Supported Extension 15 Shall be cleared to zero 14 Shall be set to one 13-6 Reserved 5 0 = General Purpose Logging feature set not supported 4 reserved 3 0 = Media Card Pass Through Command feature set not supported 2 0 = Media Serial Number not supported 1 0 = SMART self-test not supported 0 1 = SMART Error Logging not supported	4000h

85	Command and feature sets supported or enabled 15 0 = Obsolete 14 0 = NOP Command not enabled 13 0 = READ BUFFER Command not enabled 12 0 = WRITE BUFFER Command not enabled 11 Obsolete 10 0 = Host Protected Area feature set not enabled 9 0 = DEVICE RESET Command not enabled 8 0 = SERVICE Interrupt not enabled 7 0 = RELEASE Interrupt not enabled 6 0 = Look-ahead not enabled 5 0 = Write Cache not enabled 4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. 3 1 = Power Management Feature Set enabled 2 0 = Removable Media feature set not enabled 1 0 = Security Mode Feature Set not enabled 0 0 = SMART Feature Set not enabled	7008
86	Command set/feature enabled 1 5-14 0 = Reserved 13 0 = FLUSH CACHE EXT Command not supported 12 1 = FLUSH CACHE Command supported 11 0 = Device Configuration Overlay not supported 10 0 = 48-Bit Address features set not supported 9 0 = Automatic Acoustic Management feature set not enabled 8 0 = SET MAX security extension not enabled by SET MAX SETPASSWORD 7 0 = Reserved 6 0 = SET FEATURES subcommand required to spin-up after power-up not enabled 5 0 = Power-Up in Standby feature set not enabled 4 0 = Obsolete 3 1 = Advanced Power Management feature set enabled 2 0 = CFA feature set not supported 1 0 = READ/WRITE DMA QUEUED Command not supported 0 1 = DOWNLOAD MICROCODE Command supported	1004h

87	Command and feature sets supported or enabled 15 Shall be cleared to zero 14 Shall be set to one 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12 0 = Reserved for Technical Report, INCITS TR-37-2004 11 0 = Reserved for Technical Report, INCITS TR-37-2004 10:9 0 = Obsolete 8 0 = 64-Bit World Wide Name not supported 7 0 = WRITE DMA QUEUED FUA EXT Command not supported 6 0 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands not supported 5 0 = General Purpose Logging feature set not supported 4 0 = Obsolete 3 0 = Media Card Pass Through Command feature set not supported 2 0 = Media Serial Number is not valid 1 0 = SMART Self-Test not supported 0 0 = SMART Error-Logging not supported	4000h
88	Ultra DMA modes 15 Reserved 14 0 = Ultra DMA mode 6 is not supported 13 1= Ultra DMA mode 5 is selected 0= Ultra DMA mode 5 is not selected 12 1= Ultra DMA mode 4 is selected 0= Ultra DMA mode 4 is not selected 11 1= Ultra DMA mode 3 is selected 0= Ultra DMA mode 3 is not selected 10 1= Ultra DMA mode 2 is selected 0= Ultra DMA mode 2 is not selected 9 1= Ultra DMA mode 1 is selected 0= Ultra DMA mode 1 is not selected 8 1= Ultra DMA mode 0 is selected 0= Ultra DMA mode 0 is not selected 7 Reserved 6 0= Ultra DMA mode 6 is not supported 5 1= Ultra DMA mode 5 and below are supported 4 1= Ultra DMA mode 4 and below are supported 3 1= Ultra DMA mode 3 and below are supported 2 1= Ultra DMA mode 2 and below are supported 1 1= Ultra DMA mode 1 and below are supported 0 1= Ultra DMA mode 0 is supported	XX1Fh
89	Time required for Normal Erase mode SECURITY ERASE UNIT command	0000h
90	Time required for Enhanced erase mode SECURITY ERASE UNIT command	0000h
91	Current advanced power management level value	0000h

92	Master Password Identifier	0000h
93	Hardware reset result	404Fh
94	Current automatic acoustic management value 15:8 Vendor‟s recommended acoustic management value. 7:0 Current automatic acoustic management value.	0000h
95-126	Reserved	0000h
127	Obsolete	0000h
128	Security Status 15: 9 Reserved 8 Security level 0 = high, 1 = Maximum 7:6 Reserved 5 1= Enhanced security erase supported 4 1= Security count expired 3 0= Security frozen. 2 0 = Security not locked 1 0= Security not enabled 0 0= Security not supported	XXXXh
129-159	Vendor specific	XXXXh
160	CFA power mode 1	A064h
161-162	Reserved	0000h
163-164	Reserved	0012 001Bh
165-175	Reserved	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15:8 Check Sum 7:0 Signature	XXXXh

Notes:

(1) F/V = Fixed/Variable content
F = the content of the word is fixed and does not change.
V = the content of the word is variable and may be changed depending on the state of the device, commands executed.
X = the content of the word may be fixed or variable.
C = vendor specific data which can be customized before device shipping.

(2) aaaa indicates an ASCII vendor string; x indicates a numeric nibble value.

(6) Idle – 97H or E3H

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

Register	7	6	5	4	3	2	1	0
Command(7)	97h or E3h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Timer Count (5 msec increments)							
Feature(1)	X							

(7) Idle immediate – 95H or E1H

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt.

Register	7	6	5	4	3	2	1	0
Command(7)	95h or E1h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(8) Initialize Device Parameter – 91H

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Device/Head registers are used by this command.

Register	7	6	5	4	3	2	1	0
Command(7)	91h							
C/D/H(6)	X	O	X	Drive	Max Head (no. of heads-1)			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Number of sectors							
Feature(1)	X							

(9) Read Buffer – E4H

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card‟s sector buffer. This command has the same protocol as the Read Sector(s) command.

Register	7	6	5	4	3	2	1	0
Command(7)	E4h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(10) Read DMA – C8H

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 request 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, cleat BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 & sector –count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and asserts –IORD once for each 16 bit word to be transferred to the Host. Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder, head, and sector number of the sector where the occurred. The amount of data transferred is indeterminate. When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

Register	7	6	5	4	3	2	1	0
Command(7)	C8h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16							
Cylinder Low(4)	Cylinder Low (LBA 15-8							
Sector Number(3)	Sector Numbe(LBA 7-0							
Sector Count(2)	Sector Count							
Feature(1)	X							

(11) Read Long Sector – 22H or 23H

The Read Long command performs similarly to the Read Sector(s) command except that is returns 516 bytes of data instead of 512 bytes. During a Read Long command, the CompactFlash Storage Card does not check the ECC bytes to determine if there consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

Register	7	6	5	4	3	2	1	0
Command(7)	22h or 23h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	X							
Feature(1)	X							

(12) Read Sector(s) – 20H or 21H

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has buffer, sets DRQ, cleats BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder head, and sector number of the sector 2 where the error occurred. The flawed data is pending in the sector buffer.

Register	7	6	5	4	3	2	1	0
Command(7)	20h or 21h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

(13) Read Verify Sector(S) – 40H or 41H

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY. When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified. If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Register	7	6	5	4	3	2	1	0
Command(7)	40h or 41h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

(14) Recalibrate – 1XH

This command is effectively a NOP command to the CompactFlash Storage Card and is provided for compatibility.

Register	7	6	5	4	3	2	1	0
Command(7)	1Xh							
C/D/H(6)	1	LBA	1	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(15) Request Sense – 03H

Register	7	6	5	4	3	2	1	0
Command(7)	03h							
C/D/H(6)	1	LBA	1	Drive	X			
Cylinder High(5)	X							

Cylinder Low(4)	X
Sector Number(3)	X
Sector Count(2)	X
Feature(1)	X

This command requests extended error information for the previous command. Table 29 defines the valid extended error codes for the CompactFlash Storage Card Series product. The extended error code is returned to the host in the Error Register.

Table 29: Extended Error Codes

Extended Error Code	Description
01h	Self Test OK
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address
2Fh	Address Overflow
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrected ECC Error
18h	Corrected ECC Error
05h,30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error/Aborted Command
0Ch, 38h,3Bh,3Ch,3Fh	Corrupted Media Format
03h	Write/ Erase Failed
22h	Power Level 1 Disabled

(16) Seek – 7XH

This command is effectively a NOP command to the CompactFlash Storage Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

Register	7	6	5	4	3	2	1	0
Command(7)	7Xh							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	X (LBA 7-0)							

Sector Count(2)	X
Feature(1)	X

(17) Set Features – EFH

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the CompactFlash Storage Card shall return command aborted. Table 30: Feature Supported defines all features that are supported.

Register	7	6	5	4	3	2	1	0
Command(7)	EFh							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Config							
Feature(1)	Feature							

If the Sector Count Register contains a valid value and the block count is supported,the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write multiple disabled.

Table 30: Feature Supported

Feature	**Operation**
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Counter register.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft reset.
82h	Disable Write cache.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
AAh	Enable Read Look Ahead.
BBh	4 Bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

(18) Set Sleep Mode – 99H or E6H

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an

interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds.

Register	7	6	5	4	3	2	1	0
Command(7)	99h or E6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(19) Standby – 96H or E2H

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, cleat BSY and return interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

Register	7	6	5	4	3	2	1	0
Command(7)	96h or E2h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(20) Standby Immediate – 94H or E0H

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

Register	7	6	5	4	3	2	1	0
Command(7)	94h or E0h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							

Sector Number(3)	X
Sector Count(2)	X
Feature(1)	X

(21) Write Buffer– E8H

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfer 512 bytes.

Register	7	6	5	4	3	2	1	0
Command(7)	E8h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

(22) Write DMA – CAH

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512*sector count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the host asserts –DMACK while it is ready to transfer data by DMA and asserts –IOWR once for each 16 bit word to be transferred from the Host. Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The amount of data transferred is indeterminate. When a write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

Register	7	6	5	4	3	2	1	0
Command(7)	CAh							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			

Cylinder High(5)	Cylinder High (LBA 23-16)
Cylinder Low(4)	Cylinder Low(LBA 15-8)
Sector Number(3)	Sector Number (LBA 7-0)
Sector Count(2)	Sector Count
Feature(1)	X

(23) Write Sector(s) – 30H or 31H

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BST, then sets DRQ and clears BSDY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

Register	7	6	5	4	3	2	1	0
Command(7)	30h or 31h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

6.3. *SMART*

Individual SMART commands are identified by the value placed in the Feature register.

Value	Command
D0h	SMATR Read Data
D2h	SMART Enable/Disable Attribute Autosave
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS
Dah	SMART Return Status
E0h	SMART Read Remap Data

6.3.1. *SMART Enable Operation*

This command enables access to the SMART capabilities of CompactFlash Card. The state of SMART (enable or disable) is preserved across power cycles.

Register	7	6	5	4	3	2	1	0
Command(7)	B0h							
C/D/H(6)	1	1	1	Drive	X			
Cylinder High(5)	C2h							
Cylinder Low(4)	4Fh							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	D8h							

6.3.2. *SMART Disable Operation*

This command disables access to the SMART capabilities of CompactFlash Card. The state of SMART (enable or disable) is preserved across power cycles.

Register	7	6	5	4	3	2	1	0
Command(7)	B0h							
C/D/H(6)	1	1	1	Drive	X			
Cylinder High(5)	C2h							
Cylinder Low(4)	4Fh							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	D9h							

6.3.3. *SMART Enable/Disable Attribute Autosave*

This command is effectively a no-operation as the data for the SMART functionality is always available and kept current in the firmware.

Register	7	6	5	4	3	2	1	0
Command(7)	B0h							
C/D/H(6)	1	1	1	Drive	X			
Cylinder High(5)	C2h							
Cylinder Low(4)	4Fh							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	D2h							

6.3.4. *SMART Read Data*

Register	7	6	5	4	3	2	1	0
Command(7)	B0h							
C/D/H(6)	1	1	1	Drive	X			
Cylinder High(5)	C2h							
Cylinder Low(4)	4Fh							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	D0h							

This command returns one sector of SMART data. The data structure returned is:

Offset	**Value**	**Description**
0 1	04h 00h	SMART Structure Version
2..361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-Test execution status byte (Self-test completed)
364 365	00h 00h	Total time of complete off-line data collection
366	00h	-
367	00h	Off-line data collection capability (no off-line data collection)
368 369	03h 00h	SMART Capabilities
370	00h	Error logging capability (no error logging)

371	00h	-
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374..385	00h	Reserved
386..387	00h	-
388.391		Reserved
392..395		Reserved
396..510	00h	-
511		Data Structure check sum

6.3.5. *Spare Block Count Attribute*

This attributes gives information about the amount of available spare blocks.

Offset	Value	Description
0	C4h	Attribute ID-Reallocation
1 2	03h 00h	Flags –Pre-fail type, value is updated during normal operation.
3		Attribute value. The value returned here is the minimum percentage of remaining spare blocks over all flash chips.
4..5	4:Low Byte 5:High Byte	Initial number of spare blocks of the flash chip that has been used for the attribute value calculation
6..7	6:Low Byte 7:High Byte	Current number of spare blocks of the flash chip that has been used for the attribute value calculation
8..9	8:Low Byte 9:High Byte	Sum of initial number of spare blocks for all flash chips
10..11	10:Low Byte 11:High Byte	Sum of the current number of spare blocks for all flash chips

6.3.6. *Erase Count Attribute*

This attributes gives information about the amount of flash blocks that has been performed.

Offset	Value	Description
0	E5h	Attribute ID-Erase Count Usage(Vendor Specific)
1 2	02h 00h	Flags –Pre-fail type, value is updated during normal operation.
3		Attribute value. The value returned here is an estimation of the remaining card life, in percent, based on the number of block erases compared to the target number of erase cycles per flash block.
4..11		Estimated total number of blocks erases

6.3.7. *Total ECC Errors Attribute*

This attributes gives information about the total number of ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	CBh	Attribute ID-Number of ECC Error
1 2	02h 00h	Flags –Advisory type, value is updated during normal operation.
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of ECC Error(Correctable and uncorrectable)
8..11		-

6.3.8. *Correctable ECC Errors Attribute*

This attributes gives information about the total number of correctable ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	CCh	Attribute ID-Number of corrected ECC Error
1 2	02h 00h	Flags –Advisory type, value is updated during normal operation.
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of correctable ECC Error.
8..11		-

6.3.9. *Total Number of Reads Attribute*

This attributes gives information about the total number of flash read commands. This can be useful for the interpretation of the number of correctable or ECC Errors. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	E8h	Attribute ID-Number of Reads.(Vendor specific)
1 2	02h 00h	Flags –Advisory type, value is updated during normal operation.
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of flash read command.
8..11		-

6.3.10. *UDMA CRC Errors Attribute*

This attributes gives information about the total number of UDMA CRC Errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Offset	Value	Description
0	C7h	Attribute ID-UDMA CRC Error
1 2	02h 00h	Flags –Advisory type, value is updated during normal operation.
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of UDMA CRC errors.
8..11		-

6.3.11. *SMART Return Status*

This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

Register	7	6	5	4	3	2	1	0
Command(7)	B0h							
C/D/H(6)	1	1	1	Drive	X			
Cylinder High(5)	C2h							
Cylinder Low(4)	4Fh							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	Dah							

6.3.12. *SMART Read Remap Data*

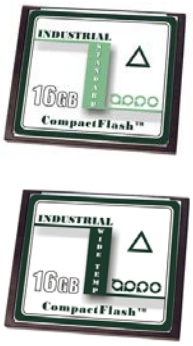
Register	7	6	5	4	3	2	1	0
Command(7)	B0h							
C/D/H(6)	1	1	1	Drive	X			
Cylinder High(5)	C2h							
Cylinder Low(4)	4Fh							
Sector Number(3)	X							
Sector Count(2)	01h							
Feature(1)	E0h							

Offset	Description
0..31	Initial number of replacement blocks for chips 0..15, 2 bytes per entry
32..63	Current number of replacement blocks for chips 0..15, 2bytes per entry
64.511	

Appendix A. Ordering Information

1. Part Number

◆ Standard Casing Industrial CF Cards supports S.M.A.R.T. function – HERMIT Series

Product Picture	Capacity	0˚ C~ 70˚ C	-40˚ C~ +85˚ C
	16MB	SPCFC016M-HACTC-UF	WPCFC016M-HAITI-UF
	32MB	SPCFC032M-HACTC-UF	WPCFC032M-HAITI-UF
	64MB	SPCFC064M-HACTC-UF	WPCFC064M-HAITI-UF
	128MB	SPCFC128M-HACTC-UF	WPCFC128M-HAITI-UF
	256MB	SPCFC256M-HACTC-UF	WPCFC256M-HAITI-UF
	512MB	SPCFC512M-HACTC-UF	WPCFC512M-HAITI-UF
	1GB	SPCFC001G-HACTC-UF	WPCFC001G-HAITI-UF
	2GB	SPCFC002G-HACTC-UF	WPCFC002G-HAITI-UF
	4GB	SPCFC004G-HACTC-UF	WPCFC004G-HAITI-UF
	8GB	SPCFC008G-HACTC-UF	WPCFC008G-HAITI-UF

◆ Rugged Metal Casing Industrial CF Cards supports S.M.A.R.T. function – HERMIT Series

Product Picture	Capacity	0˚ C~ 70˚ C	-40˚ C~ +85˚ C
	16MB	SRCFC016M-HACTC-UF	WRCFC016M-HAITI-UF
	32MB	SRCFC032M-HACTC-UF	WRCFC032M-HAITI-UF
	64MB	SRCFC064M-HACTC-UF	WRCFC064M-HAITI-UF
	128MB	SRCFC128M-HACTC-UF	WRCFC128M-HAITI-UF
	256MB	SRCFC256M-HACTC-UF	WRCFC256M-HAITI-UF
	512MB	SRCFC512M-HACTC-UF	WRCFC512M-HAITI-UF
	1GB	SRCFC001G-HACTC-UF	WRCFC001G-HAITI-UF
	2GB	SRCFC002G-HACTC-UF	WRCFC002G-HAITI-UF
	4GB	SRCFC004G-HACTC-UF	WRCFC004G-HAITI-UF
	8GB	SRCFC008G-HACTC-UF	WRCFC008G-HAITI-UF

Remarks:

1) The optional data-transfer modes and disk types are:

1. *PF: optional as PIO-4 mode / Fixed disk type*
2. *PR: optional as PIO-4 mode / Removable disk type*
3. *UF: defaulted as UDMA-4 mode / Fixed disk type*
4. *UR: optional as UDMA-4 mode / Removable disk type*
5. *AA: optional as UDMA & PIO mode Auto-detection / Fixed disk & Removable disk type Auto-detection*

2. Part Number Decoder

- **Part number construction**

X1 X2 X3 X4 X5 X6 X7 X8 X9 — X11 X12 X13 X14 X15 X16 — Z1 Z2 / C

- **Decoder Description**

X1 : Grade

S : Standard Grade – operating temperature 0º C ~ 70 º C

W : Industrial Grade – operating temperature -40º C ~ +85 ºC

X2 : The material of case

P : Plastic frame

R : Rugged metal frame

X3 X4 X5 : Product category

CFC : CompactFlash Card

X6 X7 X8 X9 : Capacity

16M:	16MB	**001G:**	1GB
32M:	32MB	**002G:**	2GB
64M:	64MB	**004G:**	4GB
128M:	128MB	**008G:**	8GB
256M:	256MB		
512M:	512MB		

X11 : Controller

H : Hyperstone (HERMIT Series)

X12 : Controller version

A, B, C, D…..

X13 : Controller Grade

C : Commercial grade

I : Industrial grade

X14 : Flash IC

T : Toshiba Flash IC

X15 : Flash IC grade / Type

C : Commercial grade

I : Industrial grade

Z1 Z2 : Data transfer rate /CF disk type

PF : PIO-6 mode / fixed disk type

PR : PIO-6 mode / removable disk type

UF : Defaulted as UDMA-4 mode / fixed disk type

UR : UDMA-4 mode / removable disk type

AA : PIO/UDMA & fixed/removable disk type auto-detected

C : Reserved for specific requirement

C : Conformal-coating

Appendix B. Limited Warranty

APRO warrants your HERMIT Series Industrial CompactFlash (CF) Card supports S.M.A.R.T. function against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

Warranty Period:

- **SLC STD. Grade 3 years / Within 60K Erasing Counts**
- **SLC IND. Grade 5 years / Within 60K Erasing Counts**

The warranty period is able to extend. Please contact APRO or Your distributor for more information.