

Nov. 2008 Rev. 1.0

Product Specification Industrial micro IDE Flash Disk (MIF) - Hermit Series -

Doc-No: 100-XMIFHA-01V0



40/44-pin Horizontal

40/44-pin Vertical

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2008/12/23

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1. Introduction

APRO Industrial 40/44-pin micro IDE Flash (MIF) Disk Hermit Series products are designed to follow ATA/ATAPI-6 standard. The main used Flash memories are Samsung SLC NAND Type Flash memory chips. The available Card capacities are 128MB, 256MB, 512MB, 1GB, 2GB, 4GB and 8GB. The operating temperature grade is optional for standard grade 0°C ~ 70°C and industrial grade -40°C ~ +85°C. The APRO Industrial 40/44-pin micro IDE Flash (MIF) Disk Hermit Series are designed electrically compliant with the conventional IDE hard disk and support True IDE Mode. The data transfer modes supports PIO mode 0~6, Multi Word DMA 0~4, or UDMA 0~5; Default setting are PIO mode-4 or UDMA-4. Hermit Series MIF features an extremely light weight, reliable, low-profile form factor.

The APRO Industrial 40/44-pin MIF Hermit Series provides a high level interface to the host computer. This interface allows a host computer to issue commands to the Flash Disk to read or write blocks of memory. The host addresses the card in 512 byte sectors. Each sector is protected by a powerful 4 bits Error Correcting Code (ECC). APRO Industrial 40/44-pin micro IDE Flash (MIF) Disk Hermit Series, it uses intelligent controller which manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management and clock control.

Figure 1 shows a block diagram of the used high tech Industrial 40/44-pin micro IDE Flash (MIF) Disk Hermit Series controller.

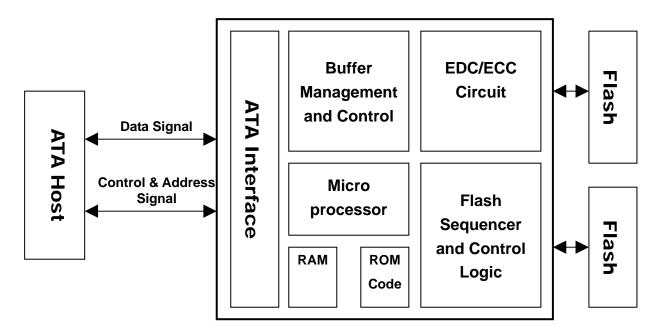


Figure 1: micro IDE Flash Disk Controller Block Diagram

1.1. Scope

This document describes the features and specifications and installation guide of APRO's Industrial 40/44-pin MIF Hermit Series. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

1.2. System Features

- Non-volatile memory and no moving parts
- SLC NAND type flash technology
- Disk capacity from 128MB to 8GB
- ATA interface and True IDE mode
- Master/Slave Switch
- Data transfer supports PIO-4 and UDMA-4 (Default setting)
- Performance up to 40.0MB/sec
- Automatic 4 bits error correction and retry capabilities
- Supports power down commands and Auto stand-by / sleep modes.
- +5 V ±10% or +3.3 V ±5% operation
- MTBF > 3,000,000 hours.
- Shock : 50g (Duration : 10ms, 3 axes), compliance to IEC 68-2-27
- Vibration : 5g (7 Hz to 2000 Hz, 3 axes), compliance to IEC 68-2-6
- Rugged environment is working well
- Very high performance, very low power consumption
- Low weight, Noiseless

1.3. ATA/ATAPI-6 Standard

APRO Industrial 40/44-pin MIF disks are fully compatible with the ATA/ATAPI-6 standard.

1.4. Technology Independence - Static Wear Leveling

In order to gain the best management for flash memory, APRO Industrial CF Cards - Hermit series supports Static

Wear Leveling technology to manage the Flash system. The life of flash memory is limited; the management is to increase the life of the flash product.

A static wear-leveling algorithm evenly distributes data over an entire Flash cell array and searches for the least used physical blocks. The identified low cycled sectors are used to write the data to those locations. If blocks are empty, the write occurs normally. If blocks contain static data, it moves that data to a more heavily used location before it moves the newly written data. The static wear leveling maximizes effective endurance Flash array compared to no wear leveling or dynamic wear leveling.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

rabio n'Ennional opernoution				
		Standard Grade	Industrial Grade	
APRO Industrial Hermit Series	MIF	SxMIFxxxx-HACSC Series	WxMIFxxx-HAISI- Series	
Temperature Operating:		0°C ~ +70°C	-40°C ~ +85°C	
	Non-operating:	-55°C ~ +95°C	-55°C ~ +95°C	
Humidity	Operating & Non-operating:	10% ~ 95% non-condensing		
Vibration	Operating & Non-operating:	5g (7 Hz to 2000 Hz, 3 axes),		
		compliance to IEC 68-2-6		
Shock	Operating & Non-operating:	50g (Duration:10ms, 3 axes),		
		compliance to IEC 68-2-27		

2.2. System Power Requirements

Table 2: Power Requirement

		Standard Grade	Industrial Grade
APRO Industrial Hermit Series MIF		SxMIFxxxx-HACSC Series	WxMIFxxx-HAISI- Series
DC Input Voltage (VCC) 100mV max. ripple(p-p)		+5 V ±10%	
	Reading Mode :	Single Channel: 69mA (max.)	/ Duel Channel: 128mA (max.)
+5V Current	Writing Mode :	Single Channel: 48mA (max.) / Duel Channel: 118mA (max.	
(Maximum average value)	Sleeping Mode :	Single Channel: 1.2mA (max.)	/ Duel Channel: 1.8mA (max.)

2.3. System Performance

Table 3: System Performances

Data Transfer Mode supporting		- PIO mode : 0,1,2,3,4,5,6 (Default PIO-4) - UDMA Mode: 0,1,2,3,4,5 (Default UDMA-4)
Data Transfer Rate To/Form Host		16.6Mybtes/sec burst under PIO Mode 4 66.6Mbytes/sec burst under UDMA-4 Mode
Average Access Time		0.2 ms(estimated)
Maria Data	Sequential Read	40 Mbytes/sec Max.
Maximum Performance	Sequential Write	17 Mbytes/sec Max.

Note:

(1). All values quoted are typically at 25oC and nominal supply voltage.

(2). Testing of the Industrial 40/44-pin micro IDE Flash (MIF) Disk Hermit Series maximum performance was performed under the following platform:

- Computer with AMD 3.0GHz processor

- Windows XP Professional operating system
- IDE transfer mode: Ultra DMA mode 4
- IDE Flash Disk capacity: 4GB

2.4. System Reliability

МТВБ	>3,000,000 hours			
Data Reliability	<1 non-recoverable error in 10 ¹⁴ bits read <1 erroneous correction in 10 ²⁰ bits read			
Wear-leveling Algorithms	Supportive			
ECC Technology	4 bits Error Connection Code			
Endurance	Greater than 2,000,000 cycles Logically contributed by Wear-leveling and advanced bad sector management			
Data Retention	10 years			

Table 4: System Reliability

2.5. Physical Specifications

Refer to Table 5 and see Figure 3 for Industrial 40/44-pin MIF physical specifications and dimensions.

rable 5. Filysical Specifications							
40-pin MIF							
Orientation : Vertical Type Horizontal Type							
Length:	60.20 mm	55.00 mm					
Width:	27.79 mm	32.40 mm					
Thickness:	6.40 mm	7.40 mm					
G. W. :	20 gw	15 gw					
44-pin MIF							
Orientation : Vertical Type Horizontal Type							
Length: 50.25 mm 48.00 mm							
Width:	32.60 mm						
Thickness: 5.80 mm 4.50 mm							
G. W. : 15 gw 10 gw							

Table 5: Physical Specifications

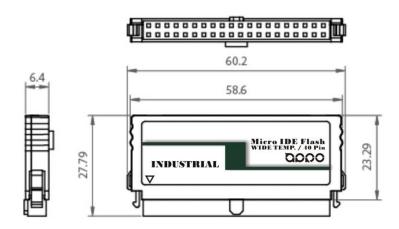


Figure 2 - 40-pin Vertical Type MIF

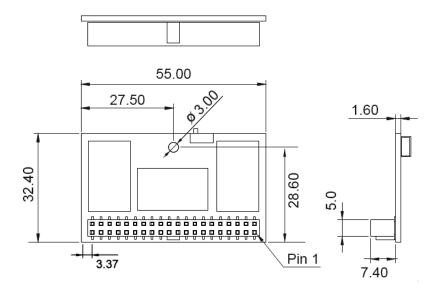


Figure 3 – 40-pin Horizontal-leftward Type MIF

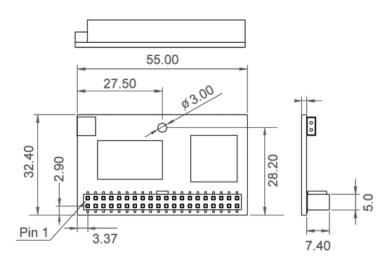


Figure 4 - 40-pin Horizontal-rightward Type MIF

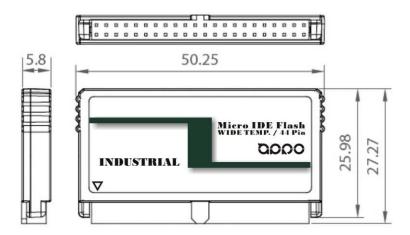
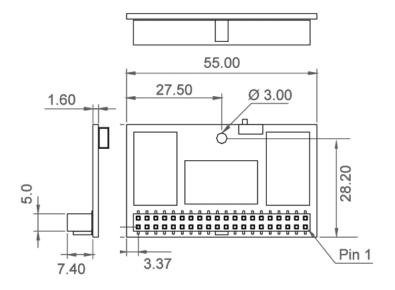


Figure 5 - 44-pin Vertical Type MIF





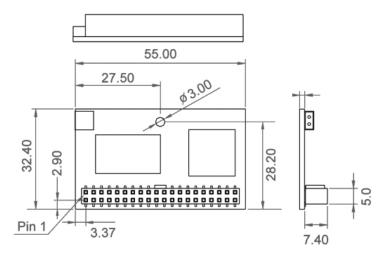


Figure 7 - 44-pin Horizontal-rightward Type MIF

2.6. Capacity Specifications

APRO Industrial 40/44-pin micro IDE Flash (MIF) Disks are built-in mainly Samsung NAND Type SLC Flash memory chips. The Table 6 shows the equipollent part number of applied Samsung Flash memory chips for each card.

Card Capacity		g SLC Flash Memory Part Number * Q'TY
	Standard Grade:	K9F1G08U0A-PCB0(1Gb) or equipollent * 1
128MB	Industrial Grade:	K9F1G08U0A-PIB0 (1Gb) or equipollent * 1
	Standard Grade:	K9F2G08U0A-PCB0 (2Gb) or equipollent * 1
		K9F1G08U0A-PCB0(1Gb) or equipollent * 2
256MB	Industrial Grade:	K9F2G08U0A-PIB0 (2Gb) or equipollent * 1
		K9F1G08U0A-PIB0 (1Gb) or equipollent * 2
	Standard Grade:	K9F4G08U0M-PCB0 (4Gb) or equipollent * 1
		K9F2G08U0A-PCB0 (2Gb) or equipollent * 2
5/015		K9F1G08U0A-PCB0(1Gb) or equipollent * 4
512MB	Industrial Grade:	K9F4G08U0M-PIB0 (4Gb) or equipollent * 1
		K9F2G08U0A-PIB0 (2Gb) or equipollent * 2
		K9F1G08U0A-PIB0 (1Gb) or equipollent * 4
	Standard Grade:	K9K8G08U0M-PCB0 (8Gb) or equipollent * 1
1GB		K9F4G08U0M-PCB0 (4Gb) or equipollent * 2
IGB	Industrial Grade:	K9K8G08U0M-PIB0 (8Gb) or equipollent * 1
		K9F4G08U0M-PIB0 (4Gb) or equipollent * 2
	Standard Grade:	K9WAG08U1M-PCB0 (16Gb) or equipollent *1
2GB		K9K8G08U0M-PCB0 (8Gb) or equipollent *2
266	Industrial Grade:	K9WAG08U1M-PIB0 (16Gb) or equipollent *1
		K9K8G08U0M-PIB0 (8Gb) or equipollent *2
	Standard Grade:	K9WAG08U1M-PCB0 (16Gb) or equipollent *2
4GB		K9K8G08U0M-PCB0 (8Gb) or equipollent *4
408	Industrial Grade:	K9WAG08U1M-PIB0 (16Gb) or equipollent *2
		K9K8G08U0M-PIB0 (8Gb) or equipollent *4
8GB	Standard Grade:	K9WAG08U1M-PCB0 (16Gb) or equipollent *4
008	Industrial Grade:	K9WAG08U1M-PIB0 (16Gb) or equipollent *4

Table 6: Card Configuration vs. Samsung NAND SLC part number

The table 7 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

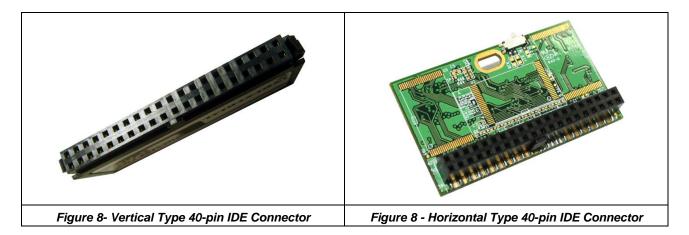
Unformatted Capacity	Default Cylinder	Default Head	Default Sector	Default CHS Capacity
128MB	500	16	32	256,000
256MB	1,000	16	32	512,000
512MB	1,015	16	63	1,023,120
1,024MB	2,031	16	63	2,047,248
2.04GB	4,063	16	63	4,095,504
4GB	8,146	16	63	8,211,168
8GB	16,000	16	63	16,128,000

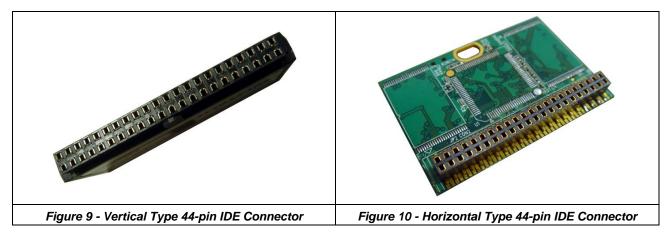
Table 7: Model Capacity

3. Interface Description

3.1. Physical Description

The pin 1 ~ pin 44 are for IDE interface.





3.2. Pin Assignments

Signals whose source is the host is designated as inputs while signals that the Industrial 44-pin micro IDE Flash (MIF) Disk sources are outputs. The pin assignments are listed in below table 8.

Table 8: Pin Assignments						
Pin No.	Signal Name	Description	Pin No.	Pin Name	Description	
1	HRESET	Host Reset	2	GND	Ground	
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8	
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9	
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10	
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11	
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12	
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13	
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14	
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15	
19	GND	Ground	20	KEY ¹	Key-pin	
21	DMARQ	DMA Request	22	GND	Ground	
	HIOW ³	Host I/O Write		0.4	GND	
23	STOP⁴	Stop Ultra DMA burst	24	24		
	HIOR ³	Host I/O Read		GND	Ground	
25	HDMARDY ⁴	Ultra DMA ready	26			
	HSTROBE ⁴	Ultra DMA data strobe				
	IORDY ³	I/O Ready				
27	DDMARDY ⁴	Ultra DMA ready	28	28	CSEL	Cable select
	DSTROBE ⁴	Ultra DMA data strobe				
29	DMACK	DMA Acknowledge	30	GND	Ground	
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit	
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic	
35	HAB[0]	Host Address Bit 0	36 HAB[2] Host Addre		Host Address Bit 2	
37	CS0	Chip Select 0	38 CS1		Chip Select 1	
39	DASP	Drive Active	40	GND	Ground	
41	VCC	Supply Voltage	42	VCC	Supply Voltage	
43 GND Ground		44 ²	NC	Not Connected		
31 33 35 37 39 41	INTRQ HAB[1] HAB[0] CS0 DASP VCC	Interrupt Request Host Address Bit 1 Host Address Bit 0 Chip Select 0 Drive Active Supply Voltage	32 34 36 38 40 42	IOCS16 PDIAG HAB[2] CS1 GND VCC	CS I/O 16-Bit Passed Diagnostic Host Address Bit 2 Chip Select 1 Ground Supply Voltage	

Table 8: Pin Assignments

In the 44-pin version, this pin is defined as KEY, according to the ATA standard.

NC = These pins are not connected internally.

Signal usage in PIO & Multiword DMA mode.

Signal usage in Ultra DMA mode.

3.3. Electrical Description

The Industrial 40/44-pin micro IDE Flash (MIF) Disk Hermit Series is optimized for operation with hosts. .Table 9: describes the signals of 40/44-pin interface.

39DASP-I/Ois present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.34PDIAG-I/OUsed as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.21DMARQODMA Request.29DMACK-IDMA Acknowledge.20 ¹ , 41 ² , 42 ² VCCVCCConnect to VCC2, 19, 22, 24,GNDGNDConnect to GND	Pin No.	Signal Name	Туре	Description			
38 CS1- I Chip select CS1 31 INTRQ O Host interrupt signal. 25 HDMARDY- ⁴ I DMA ready during Ultra DMA data in burst 23 HIOK- ³ I DMA ready during Ultra DMA data out burst 23 HIOK- ³ I I/O read strobe signal. 23 STOP ⁴ I I/O read strobe signal. 32 IOCS16- O Asserted in 16-bit access. 10RDY ³ I/O Ready Signal DMA ready during Ultra DMA data out burst 27 DDMARDY- ⁴ O DA ready during Ultra DMA data out burst 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17 I/O Host data bus 33, 35, 36 HAB[2:0] I/O Host Address bus 33, 35, 36 HAB[2:0] I/O Host Address bus 39 DASP- I/O Host as an input port to check in the slave mode to see if the slave is present or not. 34 PDIAG- I/O O DMA Request. 29 DMACK- I DMA Request. I/O MA Request. 29 DMACK- I DMA Ready during Ultra DMA data out port to return the result of diagnosis in the master. 21 DMARQ O DMA Ready during Ultra DMA data out burst 29	1	HRESET-	I	Host reset signal, High: Reset.			
31 INTRQ O Host interrupt signal. 25 HIOR. ³ I I/O read strobe signal. 23 HIOW. ³ I DMA ready during Ultra DMA data in burst 23 HIOW. ³ I I/O wite strobe signal. 32 IOCS16- O Asserted in 16-bit access. 32 IOCS16- O Asserted in 16-bit access. 10 DMARDY. ⁴ O DMA ready during Ultra DMA data out burst 11 Stop during Ultra DMA data out burst I/O write strobe signal. 32 IOCS16- O Asserted in 16-bit access. 10 DMARDY. ⁴ O DMA ready during Ultra DMA data out burst 18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17 HOB[15:0] I/O 33, 35, 36 HAB[2:0] I/O Host data bus 28 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. Switch used. 39 DASP- I/O Used as an input port to check in the master mode to see if the slave for the master is present or not. 34 PDIAG- I/O Used as an input port to check in the slave diagnosis in the master. 39 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge.	37	CS0-	I	Chip select CS0			
$\begin{array}{ c c c c } & HOR^3 & HOR^3 & HOR^3 & HOR^3 & HOR^3 & HORARDY^4 & I & DMA ready during Ultra DMA data in burst \\ \hline HSTROBE^4 & I & DMA ready during Ultra DMA data out burst & Data strobe signal. \\ \hline HOW.^3 & I & STOP^4 & I & Stop during Ultra DMA data out burst & IO write strobe signal. \\ \hline STOP^4 & O & Asserted in 16-bit access. & IORDY^3 & DDMARDY^4 & O & DMA ready during Ultra DMA data out burst & DATA data bus & STOP & DATA data out burst & DATA data bus & STOP & DATA data out burst & DATA data bus & STOP & DATA data out burst & DATA data bus & STOP & IONA data out burst & DATA data bus & STOP & IONA data out burst & DATA data bus & STOP & IONA data bus & STOP & ST$	38	CS1-	I	Chip select CS1			
25 HDMARDY. ⁴ I DMA ready during Ultra DMA data in burst 23 HIOW. ³ I Data strobe during Ultra DMA data out burst 23 HIOW. ³ I Vorite strobe signal. 32 IOCS16- O Asserted in 16-bit access. 32 IOCS16- O Asserted in 16-bit access. 707 DDMARDY. ⁴ O Asserted in 16-bit access. 10RDY ³ IORDY ³ IOR Ready Signal IOR 70 DDMARDY. ⁴ O Asserted in 16-bit access. IOR 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17 IOE[15:0] I/O Data strobe during Ultra DMA data out burst IDA 33, 35, 36 HAB[2:0] I/O Host Address bus IOR 38 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. Switch used. 39 DASP- I/O Host Address bus Ise as an input port to check in the master mode to see if the slave mode to see if the slave for the master is present or not. 34 PDIAG- I/O Used as an input port to check in the result of slave diagnosis in the master.	31	INTRQ	0	Host interrupt signal.			
HSTROBE ⁴ Data strobe during Ultra DMA data out burst 23 HIOW- ³ I I/O write strobe signal. 32 IOCS16- O Asserted in 16-bit access. 32 IOCS16- O Asserted in 16-bit access. 10RDY ³ I/O Ready Signal I/O Ready Signal 27 DDMARDY. ⁴ O DMA ready during Ultra DMA data out burst 18, 16, 14, 12, DSTROBE ⁴ O Host data bus 18, 16, 14, 12, HDB[15:0] I/O Host data bus 15, 17 HDB[15:0] I/O Host Address bus 33, 35, 36 HAB[2:0] I/O Host Address bus 28 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. Switch used. 39 DASP- I/O Used as an input port to check in the slave mode to see if the slave for the master is present or not. 34 PDIAG- I/O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC		HIOR- ³		I/O read strobe signal.			
23 HIOW. ³ I I/O write stroke signal. 32 IOCS16- O Asserted in 16-bit access. 27 IORDY ³ I/O Ready Signal I/O Ready Signal 27 DDMARDY. ⁴ O DMA ready during Ultra DMA data out burst 18, 16, 14, 12, IOS TROBE ⁴ O Host data bus 15, 7, 9, 11, 13, HDB[15:0] I/O Host data bus 33, 35, 36 HAB[2:0] I/O Host Address bus 28 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. Switch used. 39 DASP- I/O Used as an input port to check in the master mode to see if the slave for the master is present or not. 34 PDIAG- I/O Used as an input port to evaluate the result of slay ediagnosis in the master. 21 DMARQ O DMA Request. 29 DMACK- I DMA cknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC	25	HDMARDY-4	1	DMA ready during Ultra DMA data in burst			
23STOP4IStop during Ultra DMA data bursts32IOCS16-OAsserted in 16-bit access.27DDMARDY-4ODMA ready Signal27DDMARDY-4ODMA ready during Ultra DMA data out burst18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17DB[15:0]I/O33, 35, 36HAB[2:0]I/OHost data bus28CSEL-1ILow: Device operates as a master, High: Device operates as a slave. Switch used.39DASP-I/OUsed as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.21DMARQODMA Request.29DMACK-IDMA cknowledge.20', 41', 42'VCCVCCConnect to VCC2, 19, 22, 24, 2, 19, 22, 24,GNDGNDConnect to GND		HSTROBE ⁴		Data strobe during Ultra DMA data out burst			
STOP*Stop during Ultra DMA data bursts32IOCS16-OAsserted in 16-bit access.10RDY3DMARDY.4OI/O Ready Signal27DDMARDY.4ODMA ready during Ultra DMA data out burst18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17DB[15:0]I/OHost data bus33, 35, 36HAB[2:0]I/OHost Address bus28CSEL-1ILow: Device operates as a master, High: Device operates as a slave. Switch used.39DASP-I/OUsed as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.21DMARQODMA Request.29DMACK-IDMA Request.20, 14, 12, 22, 24, 2, 19, 22, 24,GNDGNDConnect to GND		HIOW- ³		I/O write strobe signal.			
IORDV ³ DDMARDY-4 O I/O Ready Signal 27 DDMARDY-4 O DMA ready during Ultra DMA data out burst 18, 16, 14, 12, INORDE4 Data strobe during Ultra DMA data in burst 10, 8, 6, 4, 3, For Strope 1 INORDE4 Data strobe during Ultra DMA data in burst 18, 16, 14, 12, INORDE4 INORDE4 Data strobe during Ultra DMA data in burst 10, 8, 6, 4, 3, For Strope 1 INORDE4 Host data bus 5, 7, 9, 11, 13, IS INORDE4 Host datas bus 33, 35, 36 HAB[2:0] INO Host Address bus 28 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. Switch used. 39 DASP- INO Used as an input port to check in the master mode to see if the slave is present or not. 34 PDIAG- INO Used as an input port to evaluate the result of slave diagnosis in the master. 21 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND	23	STOP ⁴	I	Stop during Ultra DMA data bursts			
27 DDMARDY-4 O DMA ready during Ultra DMA data out burst 18, 16, 14, 12, DSTROBE4 Data strobe during Ultra DMA data in burst 10, 8, 6, 4, 3, HDB[15:0] I/O Host data bus 33, 35, 36 HAB[2:0] I/O Host Address bus 28 CSEL-1 I Master/Slave select signal (cable select signal). 28 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. 39 DASP- I/O Used as an input port to check in the master mode to see if the slave is present or not. 34 PDIAG- I/O Used as an input port to evaluate the result of slave diagnosis in the master. 21 DMARQ O DMA Request. 29 DMACK- I DMA Request. 29 DMACK- I DMA Request. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND	32	IOCS16-	0	Asserted in 16-bit access.			
DSTROBE* Data strobe during Ultra DMA data in burst 18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17 HDB[15:0] I/O Host data bus 33, 35, 36 HAB[2:0] I/O Host Address bus 33, 35, 36 HAB[2:0] I/O Host Address bus 28 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. Switch used. 39 DASP- I/O Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave mode to see if the slave for the master is present or not. 34 PDIAG- I/O Used as an input port to evaluate the result of slave diagnosis in the master. 21 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND		IORDY ³		I/O Ready Signal			
18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17 HDB[15:0] I/O Host data bus 33, 35, 36 HAB[2:0] I/O Host Address bus 33, 35, 36 HAB[2:0] I/O Host Address bus 28 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. Switch used. 39 DASP- I/O Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not. 34 PDIAG- I/O Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master. 21 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND	27	DDMARDY-4	0	DMA ready during Ultra DMA data out burst			
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5, 7, 9, 11, 13, 15, 17HDB[15:0]I/OHost data bus33, 35, 36HAB[2:0]I/OHost Address bus33, 35, 36HAB[2:0]I/OHost Address bus28CSEL-1ILow: Device operates as a master, High: Device operates as a slave. Switch used.39DASP-I/OUsed as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.34PDIAG-I/OUsed as an input port to evaluate the result of slave diagnosis to the master.21DMARQODMA Request.29DMACK-IDMA Acknowledge.201, 41², 42²VCCVCCConnect to VCC2, 19, 22, 24, GNDGNDGNDConnect to GND	18, 16, 14, 12,						
5, 7, 9, 11, 13, Image: Constraint of the standard state of the	10, 8, 6, 4, 3,	HDB[15:0]	I/O	Host data bus			
33, 35, 36 HAB[2:0] I/O Host Address bus 33, 35, 36 HAB[2:0] I/O Host Address bus 28 CSEL-1 I Low: Device operates as a master, High: Device operates as a slave. Switch used. 39 DASP- I/O Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not. 34 PDIAG- I/O Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master. 21 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND	5, 7, 9, 11, 13,						
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Switch used.39DASP-I/OUsed as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.34PDIAG-I/OUsed as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.21DMARQODMA Request.29DMACK-IDMA Acknowledge.20 ¹ , 41 ² , 42 ² VCCVCCConnect to VCC2, 19, 22, 24,GNDGNDConnect to GND		28 CSEL- I	I	Master/Slave select signal (cable select signal).			
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39DASP-I/Ois present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.34PDIAG-I/OUsed as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.21DMARQODMA Request.29DMACK-IDMA Acknowledge.20 ¹ , 41 ² , 42 ² VCCVCCConnect to VCC2, 19, 22, 24,GNDGNDConnect to GND				Switch used.			
Markowski Markowski 34 PDIAG- 34 PDIAG- 1/O Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master. 21 DMARQ 29 DMACK- 20 ¹ , 41 ² , 42 ² VCC 20, 141 ² , 42 ² VCC 20, 19, 22, 24, GND				Used as an input port to check in the master mode to see if the slave			
34 PDIAG- I/O Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master. 21 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND	39	DASP-	I/O	is present or not, and as an output port to check in the slave mode to			
34 PDIAG- I/O master mode, and as an output port to return the result of diagnosis to the master. 21 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND				see if the slave for the master is present or not.			
21 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND				Used as an input port to evaluate the result of slave diagnosis in the			
21 DMARQ O DMA Request. 29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND	34	PDIAG-	I/O	master mode, and as an output port to return the result of diagnosis			
29 DMACK- I DMA Acknowledge. 20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND				to the master.			
20 ¹ , 41 ² , 42 ² VCC VCC Connect to VCC 2, 19, 22, 24, GND GND Connect to GND	21	DMARQ	0	DMA Request.			
2, 19, 22, 24, GND GND Connect to GND	29	DMACK-	1	DMA Acknowledge.			
GND GND GND Connect to GND	20 ¹ , 41 ² , 42 ²	VCC	VCC	Connect to VCC			
GND GND GND Connect to GND.	2, 19, 22, 24,						
26, 30, 40, 43 ²	26, 30, 40, 43 ²	GND	GND Connect to GND.		GND Connect to GND.	GND	Connect to GND.
44 ² NC N/A Not used. Please do not connect.	44 ²	NC	N/A	Not used. Please do not connect.			

Table 9: Signal Description

In the 44-pin version, this pin is defined as KEY, according to the ATA standard.

NC = These pins are not connected internally.

Signal usage in PIO & Multiword DMA mode

Signal usage in Ultra DMA mode

3.4. Electrical Specification

Table 11, Table 12, and Table 13 defines all D.C. Characteristics for the Industrial 40/44-pin micro IDE Flash (MIF) Disk Hermit Series. Unless otherwise stated, a condition is as below Table 10:

SxMIFxxxx-HACSC Series	WxMIFxxxx-HAISI- Series						
Vcch = 5V ±10% or 3.3V ± 10%	Vcch = 5V ±10% or 3.3V ± 10%						
Vccf = 3.3V ± 10%	Vccf = 3.3V ± 10%						
Ta = 0°C to 70°C	Ta = -40°C to 85°C						

Table 10: Electrical Condition

3.4.1. Absolute Maximum Rating

Table	11:	Absolute	Maximum	Rating
labic		Absolute	maximum	naung

Parameter	Symbol	Rating	Unit					
DC Power Supply	V _{DD} - V _{SS}	-0.3 ~ +5.5	V					
Input voltage	V _{IN}	V_{SS} -0.3 ~ V_{DD} +0.3	V					
Output voltage	V _{OUT}	V_{SS} -0.3 ~ V_{DD} +0.3	V					
	-	Standard: -10 ~ +70	°C					
Operating Temperature	T _A	Industrial: -40 ~ +85	°C					
	-	Standard: -55 ~ +95	°C					
Storage Temperature	Т _{st}	Industrial: -55 ~ +95	°C					

3.4.2. Recommended Operating Condition

Parameter	Symbol	Min	Тур	Max	Unit
Power Supply Voltage	Vcc	3.0	3.3	3.6	v
Input Voltage	V _{IN}	-0.3	-	Vcc+0.3	V
Power Supply for Host I/O	Vccq	3.0	-	5.5	V
Input Voltage for Host I/O	V _{IN_Host}	-0.3	-	Vccq+0.3	V

3.4.3. DC Characteristics

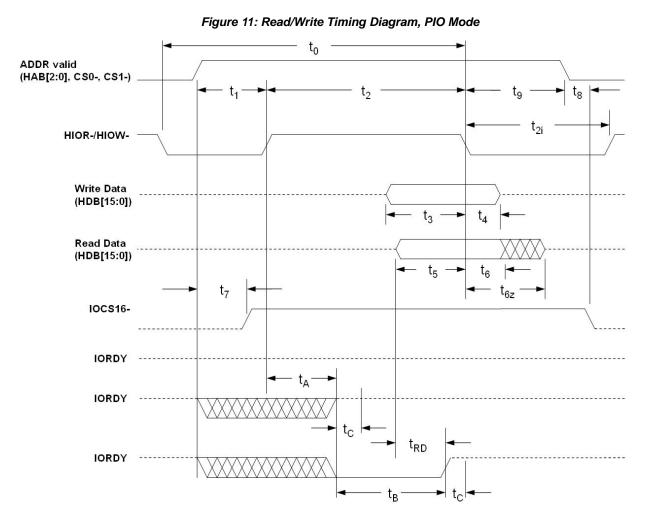
Parameter	Cumhal		11		
Parameter	Symbol	Min	Standard	Max	Unit
Power Supply	VCCH	4.5	5.0	5.5	V
Power Supply	VCCF	3.0	3.3	3.6	V
Input low voltage	V _{IL}	-0.3		0.8	V
Input high voltage	VIH	2.0		Vcc+0.3	V
Output low voltage	V _{OL}			0.45 (at	V

Table 13: DC Characteristics

			4mA)	
Output high voltage	V _{OH}	2.4 (at 1mA)		V
Operating CurrentV Sleep Mode	lcc		1.4	mA
Operation			140	mA
Input Leakage Current	ILI		±10	uA
Output leakage current	L _{LO}		±10	μA
Input/output Capacitance	CI/O		10	pF

3.4.4. Timing Specifications

PIO Mode



	PIO timing parameters	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t _o	Cycle time (min.)	600	383	240	180	120
t ₁	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25
t ₂	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70
t ₂	HIOR-/HIOW- Register 8-bit (min.)	290	290	290	80	70
t _{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25
t ₃	HIOW- data setup (min.)	60	45	30	30	20
t4	HIOW- data hold (min.)	30	20	15	10	10
t ₅	HIOR- data setup (min.)	50	35	20	20	20
t ₆	HIOR- data hold (min.)	5	5	5	5	5
t _{6z}	HIOR- data tri-state (max.)	30	30	30	30	30
t ₇	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a
t ₈	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a
t9	HIOR-/HIOW- to address valid hold	20	15	10	10	10
t _{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0
t _A	IORDY setup time	35	35	35	35	35
tв	IORDY pulse width (max.)	1250	1250	1250	1250	1250
t _c	IORDY assertion to release (max.)	5	5	5	5	5

Table 14: Read/Write Timing Specifications, PIO Mode 0-4

Multiword DMA

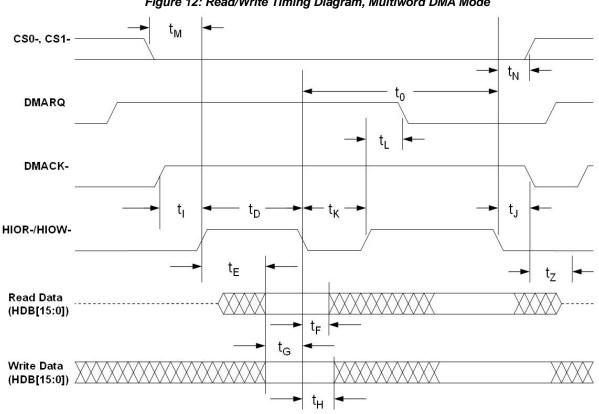


Figure 12: Read/Write Timing Diagram, Multiword DMA Mode

	Multiword DMA timing parameters	Mode 0	Mode 1	Mode 2
t _o	Cycle time (min.)	480	150	120
t _D	HIOR-/HIOW- assertion width (min.)	215	80	70
t _E	HIOR- data access (max.)	150	60	50
t⊨	HIOR- data hold (min.)	5	5	5
t _G	HIOR-/HIOW- data setup (min.)	100	30	20
t _H	HIOW- data hold (min.)	20	15	10
tı	DMACK to HIOR-/HIOW- setup (min.)	0	0	0
tJ	HIOR-/HIOW- to DMACK hold (min.)	20	5	5
t _{KR}	HIOR- negated width (min.)	50	50	25
t _{ĸw}	HIOW- negated width (min.)	215	50	25
t _{LR}	HIOR- to DMARQ delay (max.)	120	40	35
t _{LW}	HIOW- to DMARQ delay (max.)	40	40	35
tм	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25
t _N	CS1-, CS0- hold	15	10	10
tz	DMACK-	20	25	25

Table 15: Read/Write Timing Specifications, Multiword DMA Mode 0-2

Ultra DMA mode

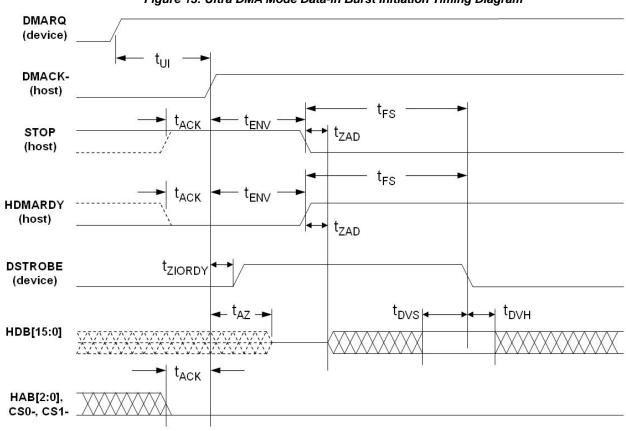


Figure 13: Ultra DMA Mode Data-in Burst Initiation Timing Diagram

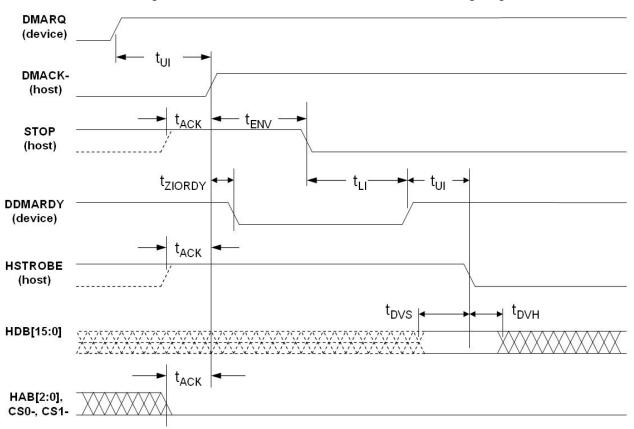
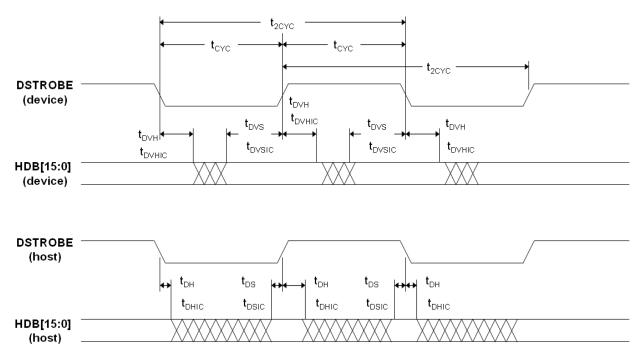


Figure 14: Ultra DMA Mode Data-out Burst Initiation Timing Diagram

Figure 15: Sustained Ultra DMA Mode Data-in Burst Timing Diagram



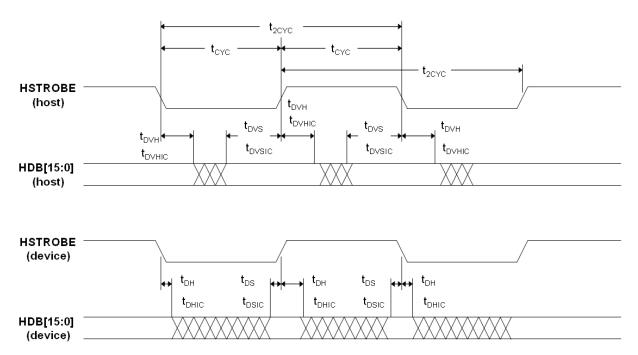


Figure 25: Sustained Ultra DMA Mode Data-out Burst Timing Diagram

Table 16: Timing Diagram, Ultra DMA Mode 0-4

Ultra DMA timing parameters		Мо	de O	Мо	de 1	Mode 2		Mode 3		Mode 4	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t _{2CYC}	Typical sustained average two cycle time	240	-	160	-	120	-	90	-	60	-
t _{cyc}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	54	-	39	-	25	-
t _{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	115	-	86	-	57	-
t _{DS}	Data setup time (at recipient)	15	-	10	-	7	-	7	-	5	-
t _{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-
\mathbf{t}_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	31	-	20	-	6.7	-
t _{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-
t _{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	170	-	130	-	120
l litra [MA timing parameters	Мо	de O	Мо	de 1	Мо	de 2	Мо	de 3	Mo	de 4
Ultra DMA timing parameters		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t∟	Limited interlock time	0	150	0	150	0	150	0	100	0	100
t _{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-
t _{ui}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-

t _{AZ}	Maximum time allowed for output drivers to	-	10	-	10	-	10	-	10	-	10
t _{zah}	release (from being asserted or negated) Minimum delay time required for output	20	-	20	-	20	-	20	-	20	-
t _{ZAD}	drivers to assert or negate (from released state)	0	-	0	-	0	-	0	-	0	-
t _{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	70	20	55	20	55
t _{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60
t _{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-
t _{iordyz}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20
t _{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-
t _{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-
t _{ss}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	20	-	20	-

4. Command Descriptions

4.1. Command Set

The following table summarizes the command defined in ATAPI-6 specification and lists the commands supported by the controller.

Command Name	Command Code
Check Power Mode	98H or E5H
Execute Device Diagnostic	90H
Erase Sector	СОН
Format Track	50H
Identify Device	ECH
Idle	97H or E3H
Idle immediate	95H or E1H
Initialize Device Parameters	91H
NOP	00H
Read Buffer	E4H
Read Long Sector	22H or 23H
Read Multiple	C4H

Read Sector	20H or 21H
Read Verify Sector	40H or 41H
Recalibrate	1XH
Seek	7ХН
Set Features	EFH
Set Multiple Mode	С6Н
Set Sleep Mode	99H or E6H
Standby	96H or E2H
Standby Immediate	94H or E0H
Write Buffer	E8H
Write Long Sector	32H or 33 H
Write Multiple	C5H
Write Sector	30H or 31H
Write Verify	ЗСН

5. Installation Procedure

5.1. Before unpacking

Before unpacking or handling a drive, take all proper electrostatic discharge (ESD) precautions, including personal and equipment grounding. Before you start to install the 40/44-pin Vertical MIF Hermit Series into your system – please check the following.

- If the shipping package appears to be damaged or water stained, notify your dealer.
- Remove the disk from its shipping enclosure and inspect it for any damage that may have occurred during shipment. If any damage is observed, notify your dealer.
- Record the disk serial number and shipment date.
- Retain the original shipping enclosure and all packing material for re-shipment.

5.2. ESD Precautions

You can prolong the life of your MIF as well as increase its reliability and prevent unnecessary damage by following the instructions listed below. Failure to follow any of these instructions may void your warranty.

- (1) Always take all proper electrostatic discharge (ESD) precautions, including personnel and equipment grounding.
- (2) Always operate the Flash disk within the environmental specifications.
- (3) Always use a grounded wrist strap when handling the Flash disk. Drives that are not installed in the system are sensitive to ESD damage.

5.3. Configuration of MIF

- (1) Select Master or Slave by Switch
- (2) Find the pin-1 of both MIF and the IDE interface on motherboard, the fool-proof device on MIF can also help to connect the IDE connector correctly.

5.4. MIF Insertion and Removing

5.4.1. MIF Insertion

The connector of V-type MIF is very tight when plugging in, and it insures the MIF connection to motherboard properly. However, you have to be very careful to insert the MIF, especially V-type MIF, in right behavior. Blows are the important points for your attention to insert the MIF.

- (1) Check the MIF housing to see if there are any damaged or loose parts and then check the female connector carefully if they are intact.
- (2) Before inserting the MIF, please check each IDE pins on motherboard are perfect and straight.

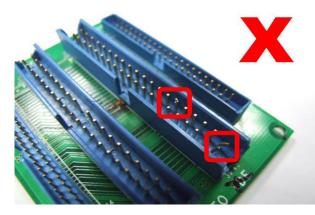


Figure 16 - Defective IDE male Pins on Motherboard



Figure 17 - Intact IDE male pins on Motherboard

(3) Any rude or wrong insertion will damage the both connectors of MIF and motherboard.



Figure 18 – Wrong Insertions

(4) When plugging in, make sure pin-1 of MIF matches to pin 1 of IDE socket on motherboard. The two ends of connectors must be vertically aligned. Press it down gently and swing slightly a few times. If insertion is not smooth, DO NOT ATTEMPT TO INSERT FORCEFULLY.

5.4.2. MIF Removing

- (1) Make sure the power is off before removing.
- (2) As they are firmly attached, you can swing gently a few times to remove. DO NOT PULL IT OFF FORECE.

5.5. IDE Device Setup / Auto-Detection

Most BIOSes have an entry in the Standard Setup menu for each of the four IDE/ATA devices supported in a system (primary master, primary slave, secondary master, and secondary slave). For each one, you can enter a value for each setting in this section (type, size, cylinders, etc.).

Virtually all BIOSes now come with IDE device Auto-Detection. This comes in two forms:

- **Dynamic IDE Auto-Detection:** This is the fully automatic mode. You set one or more of the IDE devices (primary master, primary slave, etc.) on "Auto" and the BIOS will automatically re-detect and set the correct options for the drive each time you boot the PC. The BIOS will usually display on the screen what device it finds each time it auto-detects. For most people, this is the best way to go; it ensures that your BIOS always has the correct information about your hardware, and it removes any possibility of you installing a new drive but forgetting to set up the CMOS properly, or of changing a parameter by mistake in the setup program. Not all BIOSes offer this setting but most newer ones do.
- Manual IDE Auto-Detection: This type of Auto-Detection is run from the BIOS setup program. You select Auto-Detection, and the BIOS will scan the IDE channels, and set the IDE parameters based on the devices it finds. When you save the BIOS settings, they are recorded permanently. The disadvantage of this is that if you change devices, you must return to the BIOS to re-auto-detect the new devices (unlike the dynamic Auto-Detection scheme, which does a fresh Auto-Detection each time you boot the PC). Virtually every BIOS created in the last 8 to 10 years offers manual Auto-Detection.

When you use dynamic Auto-Detection, the BIOS will normally "lock" the individual device settings that are being automatically set by the BIOS at boot time. Most systems that provide manual Auto-Detection will *not* lock the individual settings; they auto-detect, set the settings, and then let you change them if you want to. In most cases of course, you will not want to change what the BIOS detects.

Most BIOSes that allow dynamic Auto-Detection also allow manual Auto-Detection; the choice is yours. Using some sort of Auto-Detection for IDE/ATA devices is *strongly* recommended. It is the best way to reduce the chances of disk errors due to incorrect BIOS settings. It also provides immediate feedback of problems; if you can't auto-detect a drive from the BIOS, you know you have a problem even before you try to boot up.

5.6. Partition & Format

Before you install your operating system, you must first create a primary partition on the MIF on the system, and then format a file system on that partition. The Fdisk tool is an MS-DOS-based tool that you can use to prepare (partition) the MIF. You can use the Fdisk tool to create, change, delete, or display current partitions on the MIF, and then each allocated space on the MIF (primary partition, extended partition, or logical drive) is assigned a drive letter. Disk 1 may contain one extended partition, and a second MIF may contain a primary or extended partition. An extended partition may contain one or more logical MS-DOS drives.

After you use the Fdisk tool to partition MIF, use the Format tool to format those partitions with a file system. The file system File Allocation Table (FAT) allows the MIF to accept, store, and retrieve data. Windows 95 OEM Service Release 2 (OSR2), Windows 98, Windows 98 Second Edition, Windows Millennium Edition (Me), and Windows 2000 support the FAT16 and FAT32 file systems. When you run the Fdisk tool on a MIF that is larger than 512 megabytes (MB), you are prompted to choose one of the following file systems:

FAT16: This file system has a maximum of 2 gigabytes (GB) for each allocated space or drive letter. For example, if you use the FAT16 file system and have a 6-GB MIF, you can have three drive letters (C, D, and E), each with 2 GB of allocated space.

FAT32: This file system supports drives that are up to 2 terabytes in size and stores files on smaller sections of the MIF than the FAT16 file system does. This results in more free space on the MIF. The MIF file system does not support drives that are smaller than 512 MB.

When you run the **fdisk** and **format** commands, the Master Boot Record (MBR) and file allocation tables are created. The MBR and file allocation tables store the necessary disk geometry that allows MIF to accept, store, and retrieve data.

Ordering Information

X1 X2 X3 X4 X5 X6 X7 X8 X9 - X11 X12 X13 X14 X15 - Y1 Y2 Z1 / C

X1 : Grade

S: Standard Grade - operating temp. 0° C ~ 70 ° C W: Industrial Grade - operating temp. -40° C ~ 85 ° C

X2 : The material of case

B: Bare (without case)

P: Plastic case

X3 X4 X5 : Product category MIF: micro IDE Flash (module)

X6 X7 X8 X9 : Capacity

128M:	128MB
256M:	256MB
512M:	512MB
001G:	1GB
002G:	2GB
004G:	4GB
008G:	8GB

X11 : Controller

H: Hyperstone (Hermit Series)

X12 : Controller version A, B, C.....

X13 : Controller grade

C: Commercial grade I: Industrial grade

X14 : Flash IC

S: Samsung Flash IC



X15 : Flash IC grade / Type

C: Commercial grade I: Industrial grade

Y1 Y2 : MIF orient only **OV :** 40-pin IDE Vertical MIF **OR**: 40-pin IDE Right-oriented MIF OL: 40-pin IDE Left-oriented MIF 4V: 44-pin IDE Vertical MIF 4R: 44-pin IDE Right-oriented MIF 4L: 44-pin IDE Left-oriented MIF

ZI : Data transfer rate IDE interface is always Fixed Disk Mode P: PIO-4 mode

- U: UDMA-4 mode
- A: Auto PIO or UDMA mode

C : Reserved for specific requirement

C: Conformal-coating

Appendix A. Limited Warranty

APRO warrants your Industrial 40/44-pin micro IDE Flash (MIF) Disk Hermit Series against defects in material and workmanship for the life of the drive. The warranty is void in the case of misuse, accident, alteration, improper installation, misapplication or the result of unauthorized service or repair. The implied warranties of merchantability and fitness for a particular purpose, and all other warranties, expressed or implied, except as set forth in this warranty, shall not apply to the products delivered. In no event shall APRO be liable for any lost profits, lost savings or other incidental or consequential damages arising out of the use of, or inability to use, this product.

BEFORE RETURNING PRODUCT, A RETURN MATERIAL AUTHORIZATION (RMA) MUST BE OBTAINED FROM APRO.

Product shall be returned to APRO with shipping prepaid. If the product fails to conform based on customers' purchasing orders, APRO will reimburse customers for the transportation charges incurred.

After Service

1. Policy

In order to return any item for repair, an RMA (Return Merchandise Authorization) number must be assigned by APRO. Customers need to provide the following information, before an RMA will be issued:

- Product model
- Quantity
- Lot number
- Defect description
- Customer name
- Contact person
- Email address or telephone number
- Shipping address

In order to receive an RMA number, please contact our customer service department via fax or email:

- Fax the RMA Request Form to 886-2-2929 0389. The RMA Request From can be downloaded from http://www.apro-tw.com/support/rmaform.htm)
- Email to rma@apro-tw.com.tw

The description of the defect needs to be clear and complete in order for APRO to address the problem according to customer expectations. Without a clear description, APRO can only provide a basic test of the returned products.

1.1. Warranty period

- SxMIFxxxx-HACSC- Series 3 year
- WxMIFxxxx-HBISI- Series 5 years

1.2. Service charge under warranty period

For a warranty repair, there is no charge.

Remark:

The warranty does not cover product damage due to improper operation or force of nature such as fire or flood.

1.3. Service charge for out of warranty period

Out of warranty repair charges are dependent on component cost and labor time. APRO will issue an estimate after diagnosing the problem.

1.4. End of Life service

APRO cannot guarantee repair of any products beyond one year of End-of-Life due to limited availability of replacement components. If repair components are not available, APRO will suggest equivalent products for purchase and offer special pricing.

1.5. Shipping Charges

The customer is responsible for packaging the product such that no additional damage occurs during normal shipping and handling. Any freight-collect shipments without notice in advance will be refused.

For warranty repairs, the customer is responsible for the cost of shipping the product back to APRO. APRO will pay for shipping back to the customer.

For DOA warranty replacements, APRO will pay shipping charges for return and replacement. APRO reserves the right to use the most economical shipping method available.

2. Procedure

The definition of defective products fall into three categories as described below:

- DOA (Defect on Arrival): Defect occurs within 30 days of purchase.
- RMA in warranty period
- RMA out of the warranty period

The above terms are determined by the purchase date on the invoice up to the time to product is returned to APRO. APRO's repair service procedure is as follows:

2.1. Request an RMA Number from APRO:

- (1) Fill out an "RMA Request From" and send it by fax to +886-2-2929 0307 or e-mail to <u>rma@APRO</u> <u>-tw.com</u>
- APRO's RMA engineer will check that the "RAM Request From" has been completed with precise information. Then the customer will receive a RMA number.
 If you need a replacement rather than wait for the returned defective product to be repaired, this requirement must be noted in your "RMA Request From".

2.2. Package and Delivery to APRO

- (1) Returned products have to be packed properly to avoid damage during the transportation.
- (2) DOA products: DOA products qualify for complete replacement and have to be returned with all accessories included in the original purchase.

- (3) Please indicate your unique RMA umber on the top outside of the package.
- (4) To speed up the RMA/DOA procedure, please notify us by e-mail (<u>rma@APRO -tw.com</u>) with information that includes the shipping date, the name of carrier and the tracking number of the package.

2.3. Product Check On Arrival

- (1) APRO's RMA engineer will check your product within 8 hours since arrival.
- (2) If the product arrives undamaged and conforms to the conditions described on the "RMA Request Form", it will be for repairing.
- (3) If the product is damaged or there is some inconsistency with the "RMA Request Form" description, APRO will contact and confirm the status with the customer before proceeding.

2.4. Repair

- (1) The RMA engineer will repair the defect as described by the customer. The products will also be tested to ensure it is in proper working order.
- (2) If no additional problems are detected, APRO will notify the customer.
- (3) If the customer does not reply us within 48 hours, and no failure occurs during testing, the product will be processed as NTF. (No testing failure).

2.5. Charge

The customer will be charged for repairs under below conditions:

- RMA is out of the warranty period
- RMA or DOA terms apply, but it is determined by APRO's RMA engineer that the defect was caused by abuse, misuse or unauthorized repair.

2.6. Package and Delivery to the customer

- (1) We will properly pack the repaired product along with a RMA report.
- (2) The RMA number and quantity will be clearly marked on the package.
- (3) The customer will receive an e-mail notification of the product RMA number and shipping advice.