PRETEC Datasheet

Lynx Series CompactFlash Card

Preliminary version 1.1

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C-ONE Technology Corp.
8F, No.5, Lane 345, Yang Guang St., Neihu, Taipei 114-91, Taiwan R.O.C.
TEL : 02-2659-4380 FAX : 02-2659-4390 E-Mail : info@pretec.com
www.pretec.com

Document Version

Version	Description	Date	Editor	Approved by
1.0	Preliminary	2013 May	Norman Chiu	Alex Lo
1.1	Modify capacity	2013 Jul	Justin Hsu	Richard Wei

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Contents

1. Introduction

1.1 General Description

Pretec CompactFlash Card uses NAND-Type flash memory devices, which leads to its remarkable high performance and comes with capacities from 128MB to 32GB.

Compliant with ISA (Industrial Standard Architecture) bus interface standard, the CompactFlash Card performs sequential read/write for each sector (512 bytes) count. It also conforms to CompactFlash Specification and is designed with precision mechanics to enable host devices to read/write from the CompactFlash interface into Flash Media. It can operate with a 3.3V or 5V single power from the host side.

The card provides extraordinary memory medium for PC or other CF compatible electric equipments and digital still camera, and, in particular, Pretec CompactFlash Card has been approved through various compatibility tests to be used in numerous portable desktop, notebook computers and personal handheld devices such as handheld video/audio recorders, PDAs, Palm sized PCs, Handheld PCs and Auto PCs under industrial environment.

1.2 Features

- PC Card compliant
  - Conforms to CompactFlash standard 4.1
  - Compatible with PCMCIA ATA specification
  - Support CIS implemented with attribute memory
  - Compatible with all PC Card Services and Socket Services
- PCMCIA ATA / IDE interface
  - ATA command set compatible
  - Support for 8-bit or 16-bit host data transfer
- Extremely rugged and reliable
  - Advanced defect block management
  - Support background erased operation
  - Dynamic Wear-Leveling
- Power cycling test passed 3.3/5 Volt power supply, very low power consumption
  - Internal self-diagnostic program operates at V_{CC} power on
  - Auto sleep mode
- Error Correcting of 4 bits random error per sector
- Automatic on-the-fly, in-buffer Error Correcting
- Zero-power data retention, no batteries required

- 3 variations of mode access
  - Memory card mode
  - I/O card mode
  - True IDE mode
    - PIO Mode 6
    - UDMA mode 4
    - supported Multi word DMA Mode 4

1.3 Part Number Definition

$X_1X_2\,X_3\,X_4X_5\,X_6$ -X_7 X_8 X_9 X_{10}

Code	Definition	symbol	Description
X_1X_2	Card Type	CF	CF-CF card type I
X_3	Solution	Y	Lynx Series
$X_4X_5X_6$	Capacity	128	128MB
		256	256MB
		512	512MB
		01G	1GB
		02G	2GB
		04G	4GB
		08G	8GB
X_7	Temperature Range	C	Commercial Grade 0°C ~ +70°C
		H	Heavy Grade -40°C ~ +85°C
X_8	Housing	R	Metal housing
X_9X_{10}	Extension	PR	PIO 4, UDMA off, Removable
		PF	PIO 4, UDMA off, Fixed
		UR	PIO 4, UDMA 4, Removable
		UF	PIO 4, UDMA 4, Fixed

Notes:

1. Dual-Channel is xxxxxx-CP/CR/LR/HR
2. Single-Channel is xxxxxx-CPL (Only support 128MB~1GB)

2. Product Specification

2.1 Operation and environment description

Operating Voltage	DC Input Power	5V ± 10%	
		3.3V ± 5%	
Typical Power Consumptions	5V	Read Mode: TBD (Max.)	
		Write Mode: TBD (Max.)	
		Standby Mode:TBD(Approach values)	
	3.3V	Read Mode: TBD(Max.)	
		Write Mode: TBD(Max.)	
		Standby Mode: TBD(Approach values)	
Environment Conditions	Operating Temperature	Normal Temp.	0°C to +70°C
		Extended Temp.	-20°C to +85°C
		Industrial Temp.	-40°C to +85°C
		Ultra Temp.	-40°C to +125°C
	Storage Temperature	Normal Temp.	-20°C to +80°C
		Extended Temp.	-40°C to +90°C
		Industrial Temp.	-50°C to +90°C
		Ultra Temp.	-50°C to +125°C
	Humidity Operation	5% to 95% (Non-condensing)	
	Humidity Non-operation	5% to 95% (Non-condensing)	
	Shock Operation	3000-G (Max.) (duration 0.5ms, half sine wave)	
	Shock Non-operation	3000-G (Max.) (duration 0.5ms, half sine wave)	
	Vibration Operation	30-G (Peak to peak to maximum)	
	Vibration Non-operation	30-G (Peak to peak to maximum)	
Operation System Supported	DOS, Windows 98/ME/NT/2000/XP/Win7		

2.2 Physical description

Weight and Measures	Type I	Weight: 25 g Pin-Pitch: 1.27 mm	L x W x H 36.4 x 42.8 x 3.3 (mm)
Storage Capacities	Capacity		512MB – 8GB (Dual)
			128MB – 1GB (Single)
Performance	Data Transfer Rates (Dual)		Read speed up to 35 Mbytes/sec (Max.)
			Write speed up to 16 Mbytes/sec (Max.)
	Data Transfer Rates (Single)		Read speed up to 20 Mbytes/sec (Max.)
			Write speed up to 9 Mbytes/sec (Max.)
Reliability	MTBF		3,000,000 hours
	Error Correction		Error Correcting of 4 bits random error per sector
	R/W Test		Testdisk: 3,000,000 Read/Write cycles

3. Support Flash Media

3.1 Industrial CompactFlash Card Logical Format Parameters (CHS)

Card Density[*1]	128MB	256MB	512MB	1GB	2GB
Cylinder	990	993	1009	2,025	4,058
Heads	8	16	16	16	16
Sectors/Track[*2]	32	32	63	63	63
Total Sectors/Card[*3]	253,440	508,416	1,017,072	2,041,200	4,090,464
Capacity[*4]	129,341,440	259,756,032	519,913,472	1,043,234,816	2,090,893,312

Unit: Bytes

Card Density	4GB	8GB
Cylinder	8,123	16,254
Heads	16	16
Sectors/Track	63	63
Total Sectors/Card	8,187,984	16,384,032
Capacity	4,182,503,424	8,365,060,096

Unit: Bytes

Notes:

*1. It's the logical address capacity including the area which is used for file system.

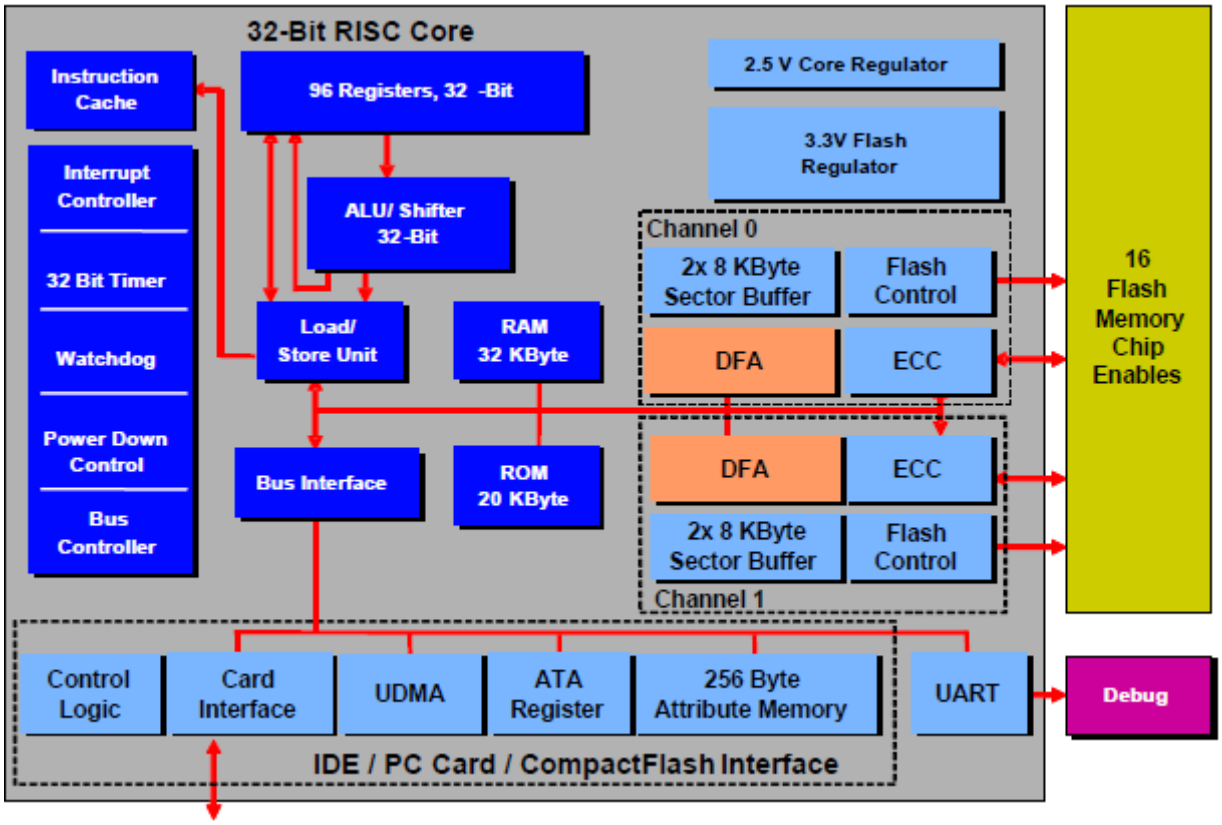
*2. Total tracks = number of head x number of cylinder.

*3. Total sector/Card = sector/track x number of head x number of cylinder.

*4. Those are general unformatted capacity of all cards.

4. Block Diagram

4.1 Controller Archive



5. Specification and Features

Electrical Specification

5.1 Recommended Operating Conditions

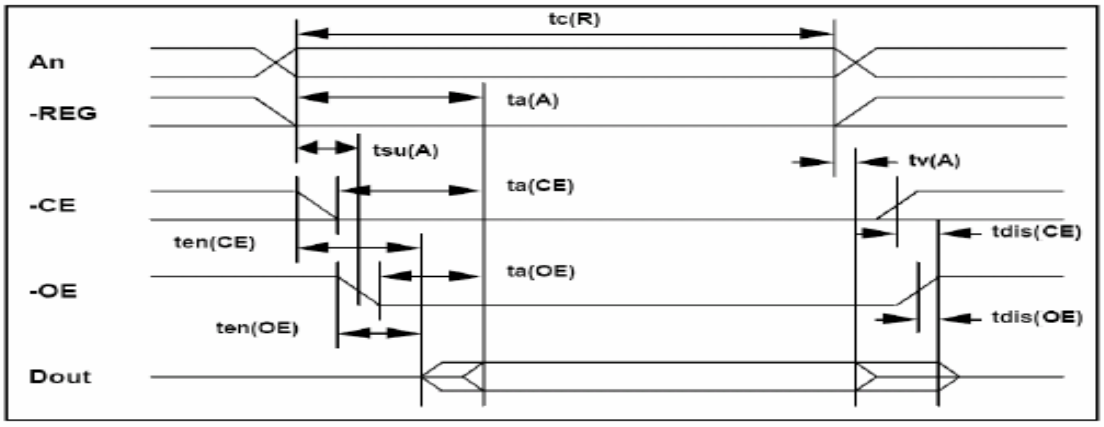
Operating Conditions	Min.	Typ.	Max.
I/O DC Supply Voltage (5V)	4.5 V	5 V	5.5 V
I/O DC Supply Voltage (3.3V)	3.0 V	3.3 V	3.6 V
Temperature	-40°C	25°C	85°C

5.2 DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input LOW Voltage	-0.3	+0.8	V	
V_{IH}	Input HIGH Voltage	2.0	VCC+0.3	V	
V_{OL}	Output LOW Voltage		0.45	V	at 4mA(12mA for DASP)
V_{OH}	Output HIGH Voltage	2.4		V	at 1mA
I_{CC}	Operating Current Sleep mode Operating, 20MHZ Operating, 40MhZ		 0.35 45 80	 mA mA mA	 Typical 0.2mA Typical 30mA Typical 50mA
I_{LI}	Input Leakage Current		±10	μA	If not pull-up / pull-down
I_{LO}	Output Leakage Current		±10	μA	
$C_{I/O}$	Input/Output Capacitance		2.0	pF	

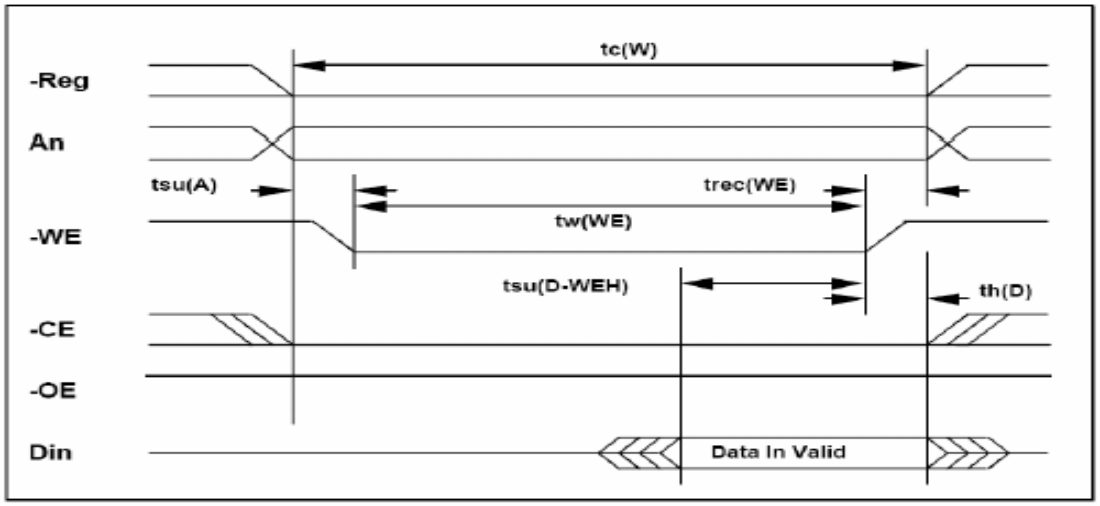
5.3 Attribute Memory Read Timing Specification

Item	Symbol	IEEE Symbol	Min.(ns)	Max. (ns)
Read Cycle Time	tc(R)	tAVAV	250	-
Address Cycle Time	ta(A)	tAVQV	-	250
Card Enable Access Time	ta(CE)	tELQV	-	250
Output Enable Access Time	ta(OE)	tGLQV	-	125
Output Disable Time from CE	tdis(CE)	tEHQZ	-	100
Output Disable Time from OE	tdis(OE)	tGHQZ	-	100
Address Setup Time	tsu (A)	tAVGL	30	-
Output Enable Time from CE	ten(CE)	tELQNZ	5	-
Output Enable Time from OE	ten(OE)	tGLQNZ	5	-
Data Valid from Address Change	tv(A)	tAXQX	0	-



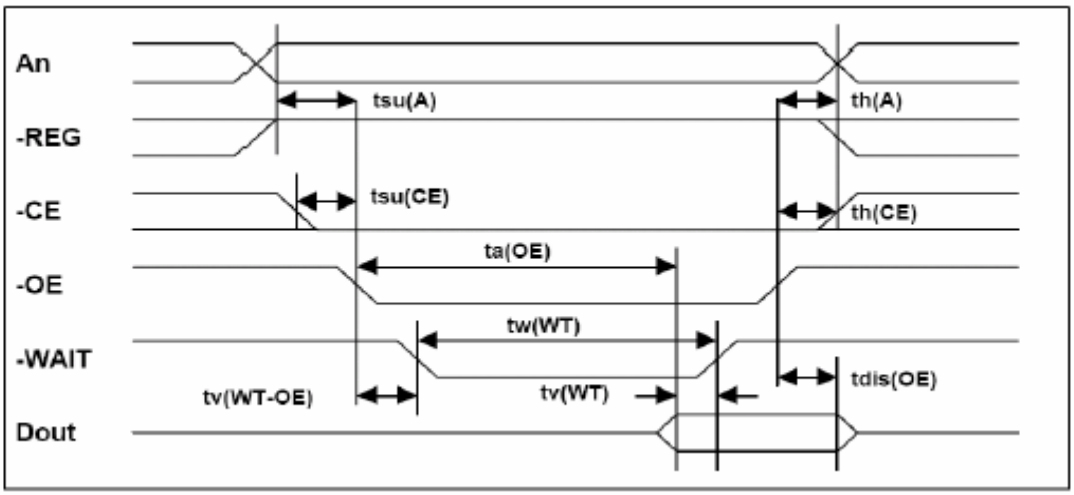
5.4 Configuration Register (Attribute Memory) Write Timing Specification

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Write Cycle Time	tc(W)	tAVAV	250	-
Write Pulse Width	tw(WE)	tWLWH	150	-
Address Setup Time	tsu(A)	tAVWL	30	-
Write recovery time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	-
Data Hold Time	th(D)	tWMDX	30	-



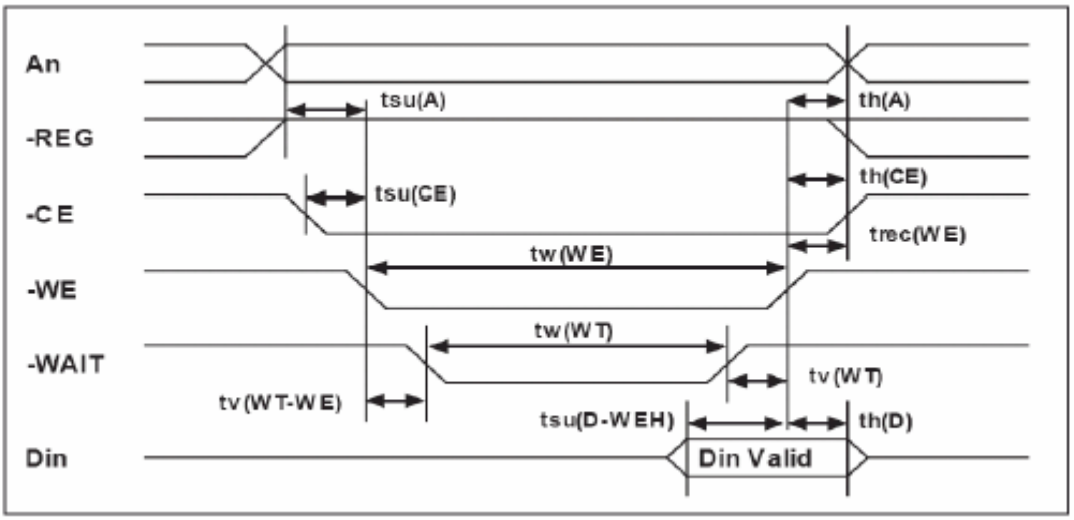
5.5 Common Memory Read Timing Specification

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Output Enable Access Time	ta(OE)	tGLQV	-	45
Output Disable Time from OE	tdis(OE)	tGHQZ	-	45
Address Setup Time	tsu(A)	tAVGL	10	-
Address Hold Time	th(A)	tGHAX	10	-
CE Setup before OE	tsu(CE)	tELGL	0	-
CE Hold following OE	th(CE)	tGHEH	10	-
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV	-	35
Data Setup for Wait Release	tv(WT)	tQVWTH	-	0
Wait Width Time	tw(WT)	tWTLWTH	-	350 (3000 for CF+)



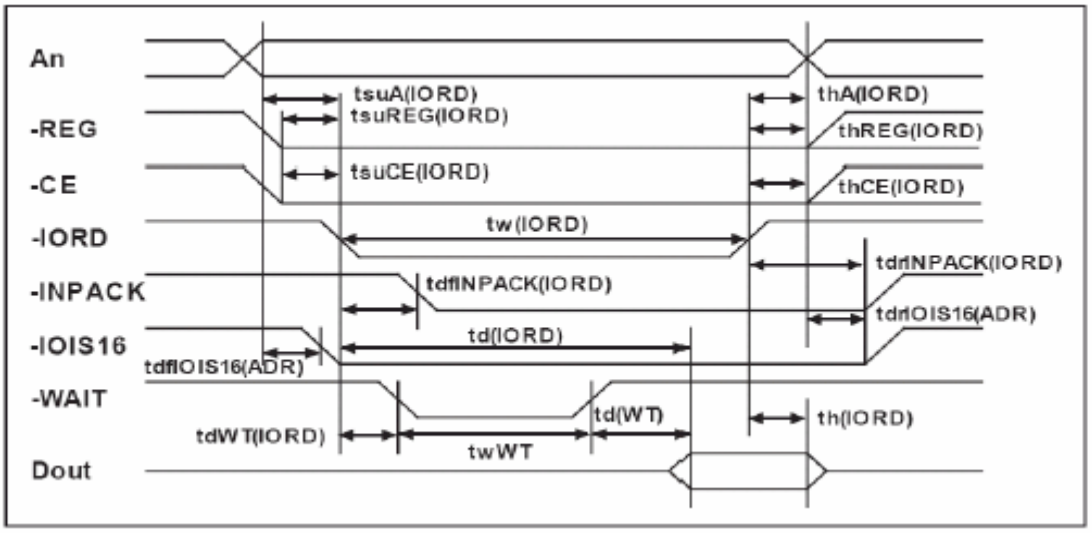
5.6 Common Memory Write Timing Specification

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before WE	tsu(D-WEH)	tDVWH	30	-
Data Hold following WE	th(D)	tWMDX	10	-
WE Pulse Width	tw(WE)	tWLWH	55	-
Address Setup Time	tsu(A)	tAVWL	10	-
CE Setup before WE	tsu(CE)	tELWL	0	-
Write Recovery Time	trec(WE)	tWMAX	30	-
Address Hold Time	th(A)	tGHAX	10	-
CE Hold following WE	th(CE)	tGHEH	10	-
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV	-	35
WE High from Wait Release	tv(WT)	tWTHWH	0	-
Wait Width Time	tw (WT)	tWTLWTH	-	350 (3000 for CF+)



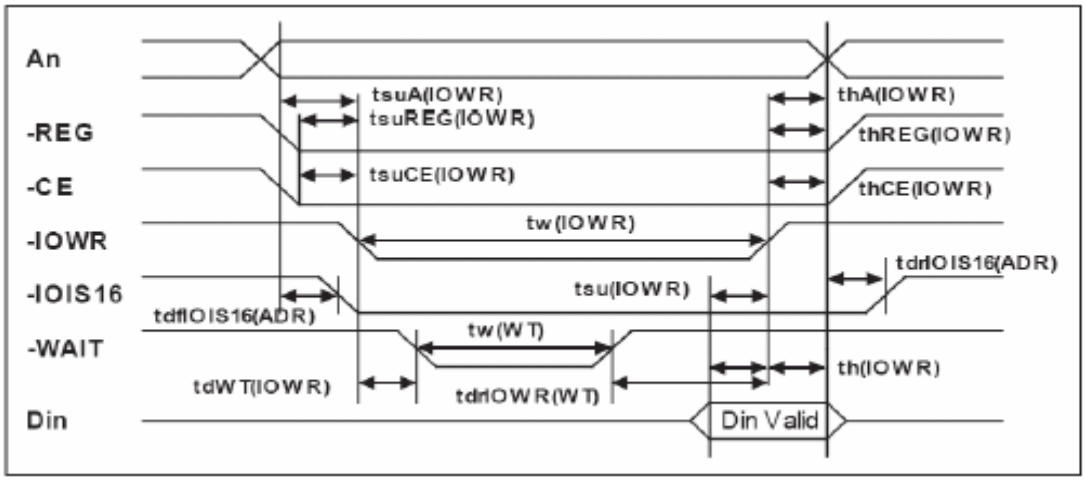
5.7 I/O Input (Read) Timing Specification

Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Data Delay after IORD	td(IORD)	tIGLQV	-	45
Data Hold following IORD	th(IORD)	tIGHQX	5	-
IORD Width Time	tw(IORD)	tIGLIGH	55	-
Address Setup before IORD	tsuA(IORD)	tAVIGL	15	-
Address Hold following IORD	thA(IORD)	tIGHAX	10	-
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	-
CE Hold following IORD	thCE(IORD)	tIGHEH	10	-
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	-
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	-
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH	-	45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL	-	35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH	-	35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL	-	35
Data Delay from Wait Rising	td(WT)	tWTHQV	-	0
Wait Width Time	tw(WT)	tWTLWTH	-	350 (3000 for CF+)



5.8 I/O Input (Write) Timing Specification

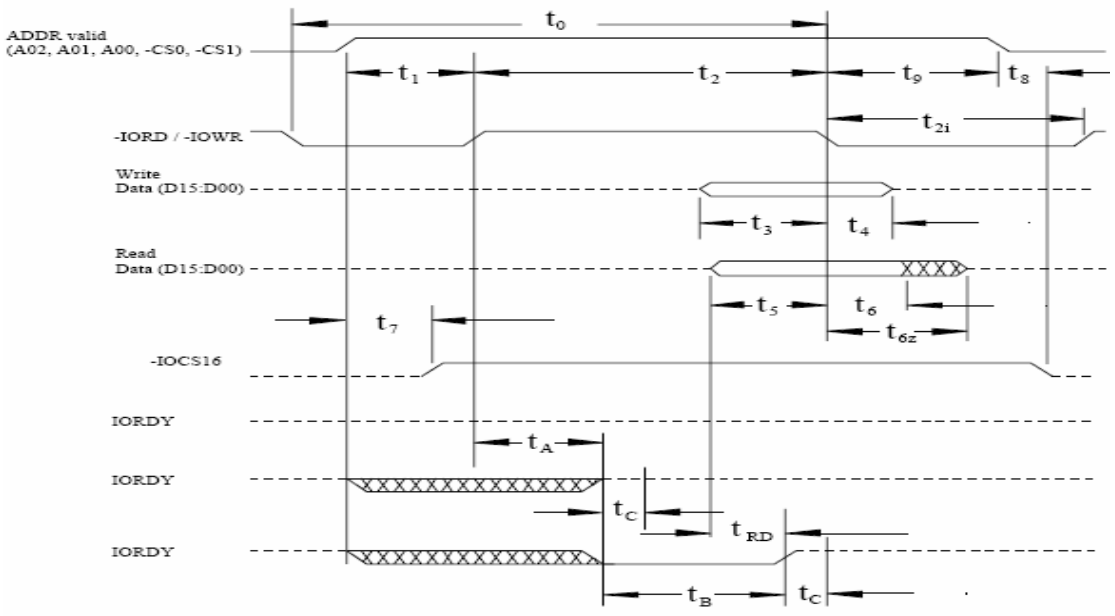
Item	Symbol	IEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH	15	-
Data Hold following IOWR	th(IOWR)	tIWHDX	5	-
IOWR Width Time	tw(IOWR)	tIWLIWH	55	-
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	15	-
Address Hold following IOWR	thA(IOWR)	tIWHAX	10	-
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	-
CE Hold following IOWR	thCE(IOWR)	tIWHEH	10	-
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	-
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0	-
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL	-	35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH	-	35
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL	-	35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	-
Wait Width Time	tw(WT)	tWTLWTH	-	350



5.9 True IDE Mode PIO (Read/Write) Timing Specification

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	
t1	Address Valid to -IORD/-IOWR setup (min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	
t2	-IORD/-IOWR (min) Register (8 bit)	290	290	290	80	70	65	55	
t2i	-IORD/-IOWR recovery time (min)	-	-	-	70	25	25	20	
t3	-IOWR data setup (min)	60	45	30	30	20	20	15	
t4	-IOWR data hold (min)	30	20	15	10	10	5	5	
t5	-IORD data setup (min)	50	35	20	20	20	15	10	
t6	-IORD data hold (min)	5	5	5	5	5	5	5	
t6Z	-IORD data tristate (max)	30	30	30	30	30	20	20	
t7	Address valid to -IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a	
t8	Address valid to -IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a	
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na	na	
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na	na	
tC	IORDY assertion to release (max)	5	5	5	5	5	na	na	

5.10 True IDE PIO Mode Timing Diagram



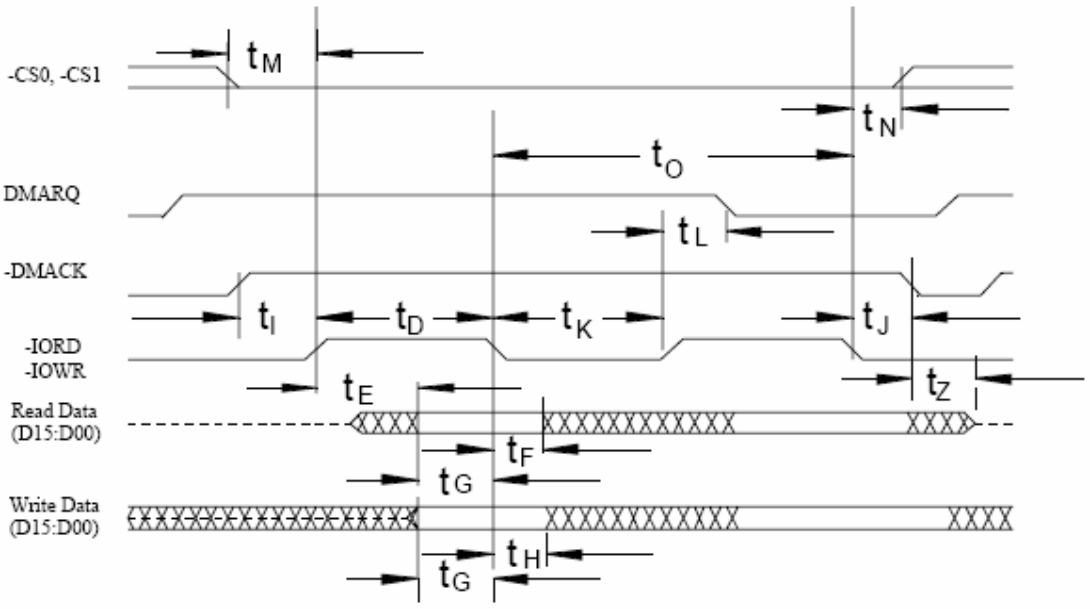
5.11 True IDE Multiword DMA Mode I/O (Read/Write) Timing

Specification

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)
t_O	Cycle time (min)	480	150	120	100	80
t_D	-IORD / -IOWR asserted width (min)	215	80	70	65	55
t_E	-IORD data access (max)	150	60	50	50	45
t_F	-IORD data hold (min)	5	5	5	5	5
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10
t_H	-IOWR data hold (min)	20	15	10	5	5
t_I	DMACK to –IORD/-IOWR setup (min)	0	0	0	0	0
t_J	-IORD / -IOWR to -DMACK hold (min)	20	5	5	5	5
t_{KR}	-IORD negated width (min)	50	50	25	25	20
t_{KW}	-IOWR negated width (min)	215	50	25	25	20
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5
t_N	CS(1:0) hold	15	10	10	10	10
t_Z	-DMACK	20	25	25	25	25

5.12 True IDE Multiword DMA Mode Read/Write Timing

Diagram



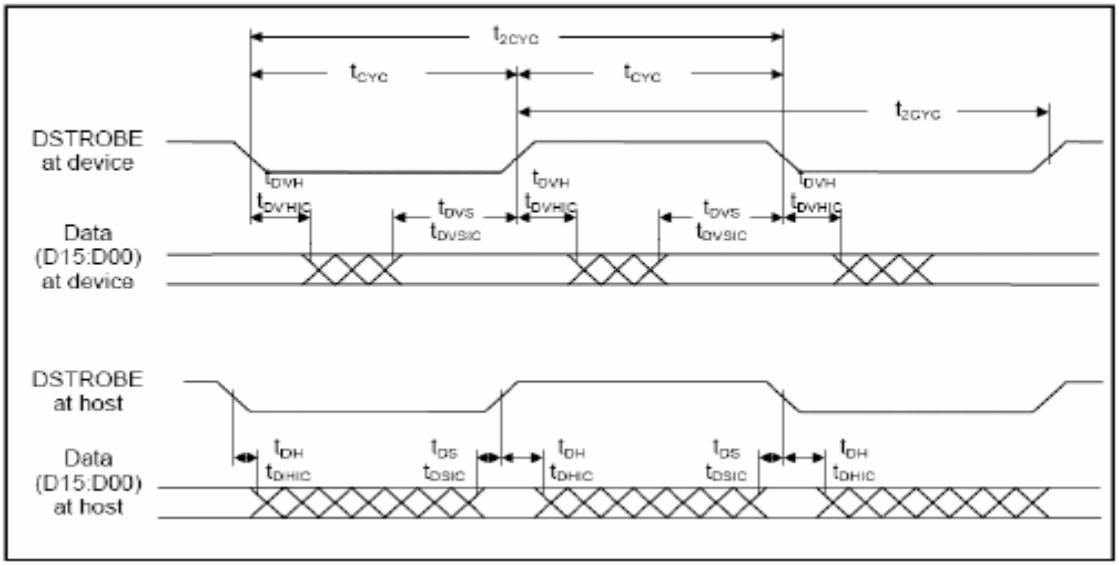
5.13 Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0 (in ns)		UDMA Mode 1 (in ns)		UDMA Mode 2 (in ns)		UDMA Mode 3 (in ns)		UDMA Mode 4 (in ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
$t_{2CYCTYP}$	240		160		120		90		60	
t_{CYC}	112		73		54		39		25	
t_{2CYC}	230		153		115		86		57	
t_{DS}	15.0		10.0		7.0		7.0		5.0	
t_{DH}	5.0		5.0		5.0		5.0		5.0	
t_{DVS}	70.0		48.0		31.0		20.0		6.7	
t_{DVH}	6.2		6.2		6.2		6.2		6.2	
t_{CS}	15.0		10.0		7.0		7.0		5.0	
t_{CH}	5.0		5.0		5.0		5.0		5.0	
t_{CVS}	70.0		48.0		31.0		20.0		6.7	
t_{CVH}	6.2		6.2		6.2		6.2		6.2	
t_{ZFS}	0		0		0		0		0	
t_{DZFS}	70.0		48.0		31.0		20.0		6.7	
t_{FS}		230		200		170		130		120
t_{LI}	0	150	0	150	0	150	0	100	0	100
t_{MLI}	20		20		20		20		20	
t_{UI}	0		0		0		0		0	
t_{AZ}		10		10		10		10		10
t_{ZAH}	20		20		20		20		20	
t_{ZAD}	0		0		0		0		0	
t_{ENV}	20	70	20	70	20	70	20	55	20	55
t_{RFS}		75		70		60		60		60
t_{RP}	160		125		100		100		100	
t_{IORDYZ}		20		20		20		20		20
t_{ZIORDY}	0		0		0		0		0	
t_{ACK}	20		20		20		20		20	
t_{SS}	50		50		50		50		50	

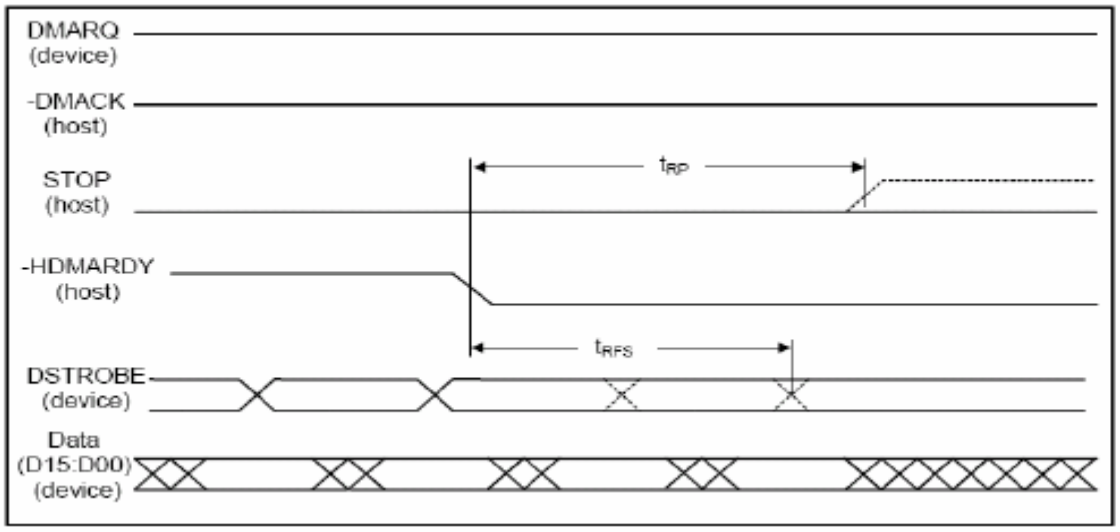
5.14 Ultra DMA Data Burst Timing Descriptions

Name	Comment
$t_{2CYCTYP}$	Typical sustained average two cycle time
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)
t_{CS}	CRC word setup time at device
t_{CH}	CRC word hold time device
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
t_{LI}	Limited interlock time
t_{MLI}	Interlock time with minimum
t_{UI}	Unlimited interlock time
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)
t_{ZAH}	Minimum delay time required for output
t_{ZAD}	drivers to assert or negate (from released)
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)
t_{IORDYZ}	Maximum time before releasing IORDY
t_{ZIORDY}	Minimum time before driving IORDY
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

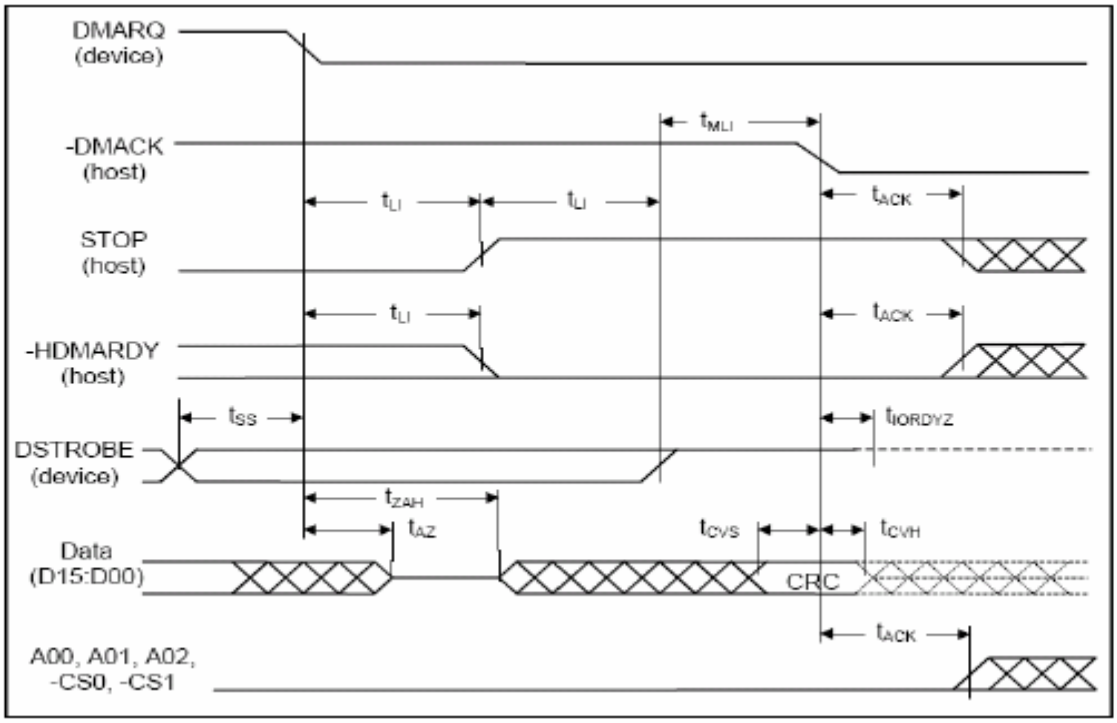
5.15 Sustained Ultra DMA Data-In Burst Timing



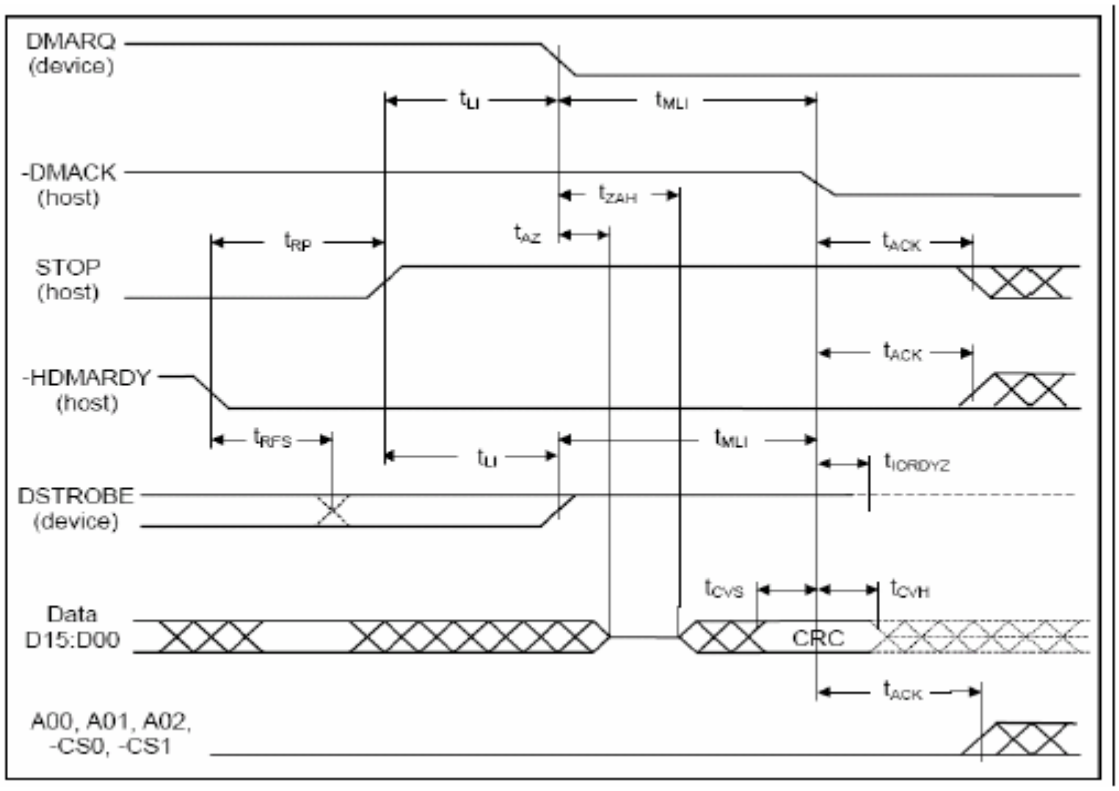
5.16 Ultra DMA Data-In Burst Host Pause Timing



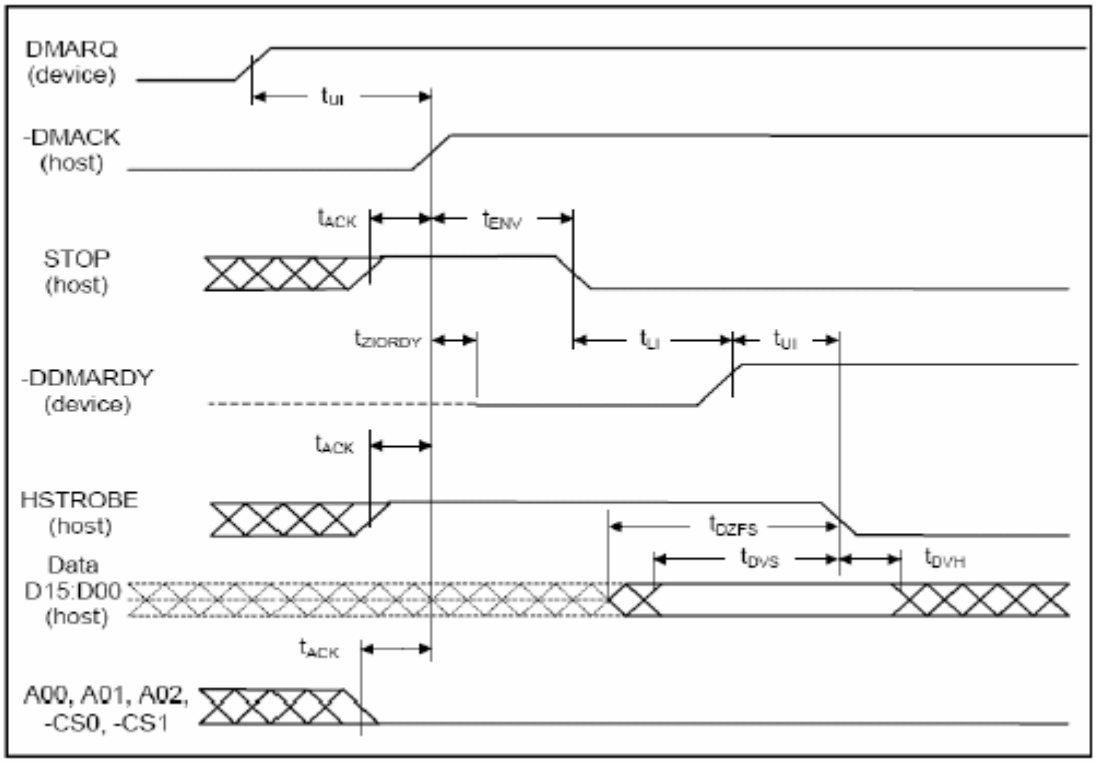
5.17 Ultra DMA Data-In Burst Device Termination Timing



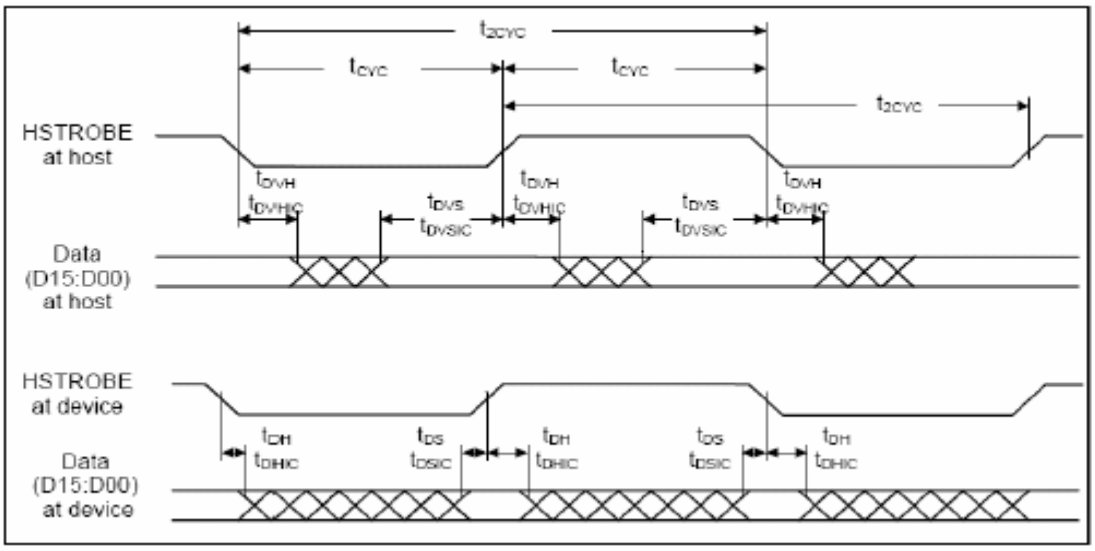
5.18 Ultra DMA Data-In Burst Host Termination Timing



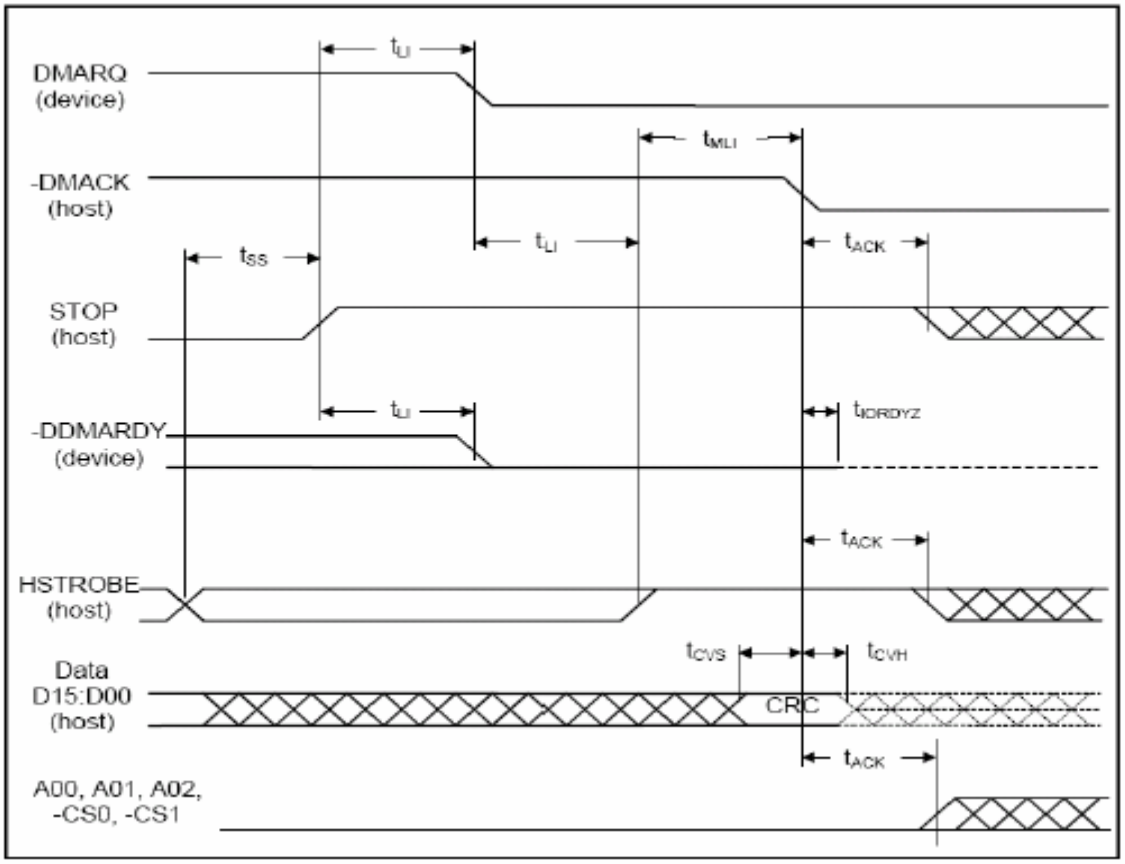
5.19 Ultra DMA Data-Out Burst Host Initiation Timing



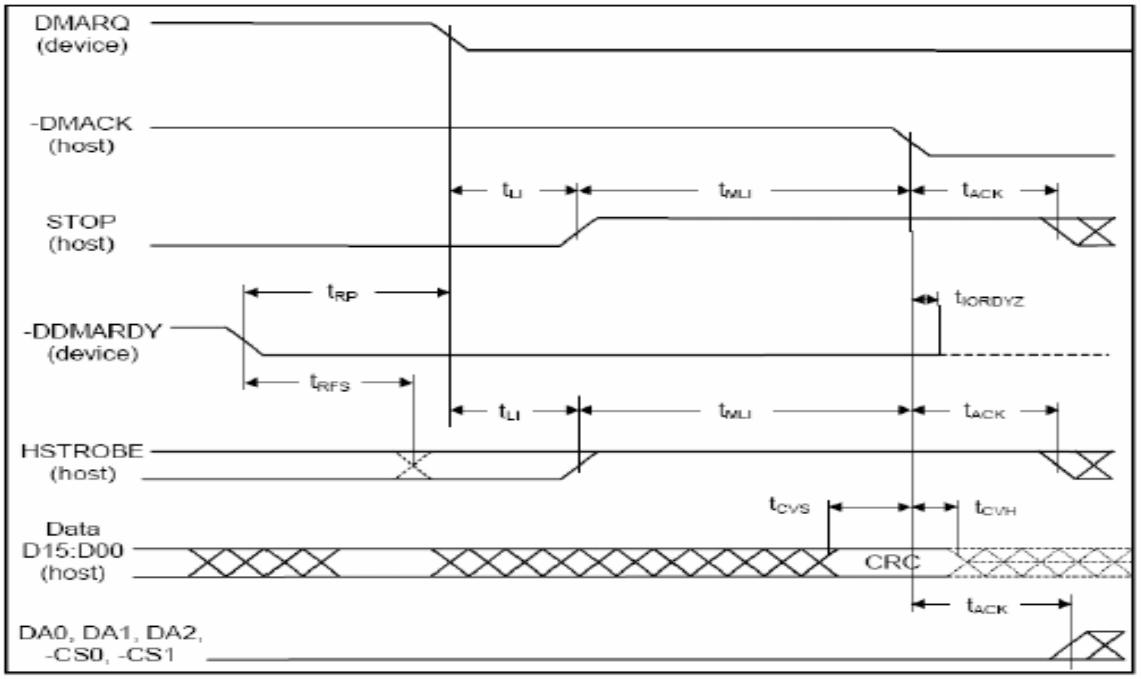
5.20 Sustained Ultra DMA Data-Out Burst Timing



5.21 Ultra DMA Data-Out Burst Host Termination Timing

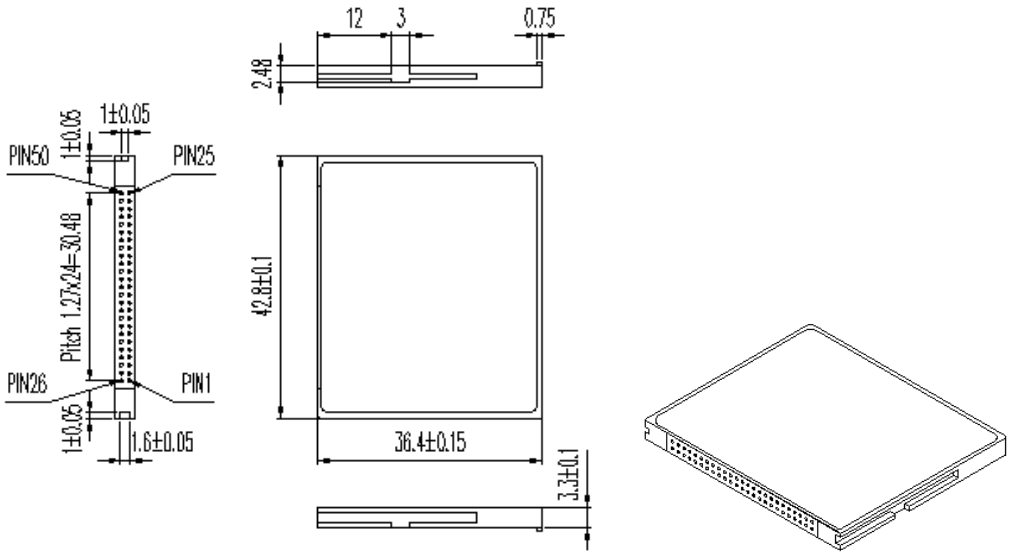


5.22 Ultra DMA Data-Out Burst Device Termination Timing



6. Physical Specification

6.1 CompactFlash Card Type



6.2 Pin Assignment

6.2.1 CompactFlash Pin Type

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
No.	Pin Name	I/O	No.	Pin Name	I/O	No.	Pin Name	I/O
1	GND	-	1	GND	-	1	GND	-
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	CE1#	I	7	CE1#	I	7	CS0#	I
8	A10	I	8	A10	I	8	A10	I
9	OE#	I	9	OE#	I	9	ATASEL#	I
10	A09	I	10	A09	I	10	A09	I
11	A08	I	11	A08	I	11	A08	I
12	A07	I	12	A07	I	12	A07	I
13	VCC	-	13	VCC	-	13	VCC	-
14	A06	I	14	A06	I	14	A06	I
15	A05	I	15	A05	I	15	A05	I
16	A04	I	16	A04	I	16	A04	I
17	A03	I	17	A03	I	17	A03	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	IOIS16#	O	24	IOCS16#	O
25	CD2#	O	25	CD2#	O	25	CD2#	O
26	CD1#	O	26	CD1#	O	26	CD1#	O
27	D11	I/O	27	D11	I/O	27	D11	I/O
28	D12	I/O	28	D12	I/O	28	D12	I/O
29	D13	I/O	29	D13	I/O	29	D13	I/O
30	D14	I/O	30	D14	I/O	30	D14	I/O
31	D15	I/O	31	D15	I/O	31	D15	I/O
32	CE2#	I	32	CE2#	I	32	CS1#	I
33	VS1#	O	33	VS1#	O	33	VS1#	O
34	IORD#	I	34	IORD#	I	34	IORD#	I
35	IOWR#	I	35	IOWR#	I	35	IOWR#	I
36	WE#	I	36	WE#	I	36	WE#	I
37	RDY/BSY#	O	37	IREQ	O	37	INTRQ	O
38	VCC	-	38	VCC	-	38	VCC	-
39	CSEL#	I	39	CSEL#	I	39	CSEL#	I

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
40	VS2#	O	40	VS2#	O	40	VS2#	O
41	RESET	I	41	RESET	I	41	RESET#	I
42	WAIT#	O	42	WAIT#	O	42	IORDY	O
43	INPACK#	O	43	INPACK#	O	43	RFU*1	O
44	REG#	I	44	REG#	I	44	RFU	I
45	BVD2	I/O	45	SPKR#	I/O	45	DASP#	I/O
46	BVD1	I/O	46	STSCHG#	I/O	46	PDIAG#	I/O
47	D08	I/O	47	D08	I/O	47	D08	I/O
48	D09	I/O	48	D09	I/O	48	D09	I/O
49	D10	I/O	49	D10	I/O	49	D10	I/O
50	GND	-	50	GND	-	50	GND	-

Notes:

1. RFU is reserved for feature use.

6.2.2 Signal Description

Signal Name	Description	I/O	Pin
VCC (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	5V , 3.3V	-	13,38
GND (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	Ground.	-	1,50
A0-A10 (PC Card Memory Mode)	These address lines along with the #REG signal are used to select the I/O port address registers within the card, the memory mapped port address registers within the Card, a byte in the card's information structure and its configuration control and status registers.	I	8,10,11,12, 14,15,16,17, 18,19,20
A0-A10 (PC Card I/O Mode)	This signal is the same as the PC Card Memory Mode signal.		-
A0-A10 (True IDE Mode)	In True IDE Mode only A0-A2 are used to select the one of eight registers in the ATA Task File, the other address lines should be grounded.	-	-
D0-D15 (PC Card Memory Mode) (PC Card I/O Mode)	These lines carry the Data, Commands and Status between the host and controller. D00 is the LSB of the even byte of the word. D08 is the LSB of the odd byte of the word.	I/O	2,3,4,5,6, 21,22,23,27, 28,29,30,31, 47,48,49
D0-D15 (True IDE Mode)	In True IDE Mode, all Task File operations occur in the byte mode on the low order D00-D07 while all data transfers are 16 bits using D00-D15.	-	-

CD1#, CD2# (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	These Card Detect pins are connected to ground on this card and used by the host to determine that the card is fully inserted into the socket.	O	25,26
VS1#,VS2# (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	Voltage Sense Signals.	O	33,40
CSEL# (PC Card Memory Mode)	This signal is not used for this mode.	I	39
CSEL# (PC Card I/O Mode)	This signal is not used of this mode.	-	-
CSEL# (True IDE Mode)	This internally pulled up signal is used to configure this card as a Master or a Slave. When this pin is grounded, this card is Master. When this pin is open, this card is Slave.	-	-
CE1#,CE2# (PC Card Memory Mode) (PC Card I/O Mode)	These signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. #CE2 always accesses the odd byte of the word. #CE1 accesses the even byte or the odd byte of the word depending on A0 and #CE2.	I	7,32
CS0#, CS1# (True IDE Mode)	In the True IDE Mode, #CS0 is the chip select for the Task File Registers while #CS1 is used to select the Alternate Status and the Device Control Register.	-	-
BVD1 (PC Card Memory Mode)	This signal is asserted high as the BVD1 signal since a battery is not used with this card.	I/O	46
STSCHG# (PC Card I/O Mode)	This signal is asserted low to alert the host to changes in the RDY/#BSY and Write Protect states, while the I/O interface is configured. The Card Configure and Status Register will control it.	-	-
PDIAG# (True IDE Mode)	In the True IDE Mode, this I/O is the Pass Diagnostic signal in the Master/Slave handshake protocol.	-	-
BVD2 (PC Card Memory Mode)	This signal is always driven to a high state in Memory Mode since a battery is not required for this card.	I/O	45
SPKR# (PC Card I/O Mode)	This signal is always driven to a high state in I/O Mode since this card does not support the audio function.	-	-
DASP# (True IDE Mode)	In the True IDE Mode, this I/O is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.	-	-
OE# (PC Card Memory Mode)	This is an Output Enable Strobe generated by the host interface. It is used to read data from the card in Memory Mode and to read CIS and configuration registers.	I	9

Signal Name	Description	I/O	Pin
OE# (PC Card I/O Mode)	In I/O Mode, this signal is used to read the CIS and configuration registers.	-	-
|ATASEL# (True IDE Mode)	To enable True IDE Mode, this signal should be grounded.	-	-
RESET (PC Card Memory Mode)	When the signal is high, the signal Resets the card.	I	41
RESET (PC Card I/O Mode)	When the signal is high, the signal Resets the card.	-	-
RESET# (True IDE Mode)	In the True IDE Mode, the signal is the active low hardware reset from the host.	-	-
REG# (PC Card Memory Mode)	This signal is used during Memory Cycle to distinguish between Common Memory and Attribute Memory accesses. High for Common Memory and Low for Attribute Memory.	I	44
REG# (PC Card I/O Mode)	This signal must be low during I/O Cycles when the I/O address is on the Bus.	-	-
RFU (True IDE Mode)	In the True IDE Mode, this signal is not used and should be connected to VCC by the host.	-	-
WE# (PC Card Memory Mode)	This signal is driven by the host and used for generating memory write cycle to the registers of the card when the card is configured in the Memory mode.	I	36
WE# (PC Card I/O Mode)	In I/O mode, this signal is used for writing the configuration registers.	-	-
WE# (True IDE Mode)	In the True IDE Mode, this signal is not used and should be connected to VCC by the host.	-	-
WAIT#(PC Card Memory Mode) (PC Card I/O Mode)	This signal is driven low by the card to notify the host to delay completion of the memory of I/O cycle that is in progress.	O	42
IORDY (True IDE Mode)	In the True IDE Mode, this signal may be used as IORDY.	-	-
INPACK# (PC Card Memory Mode)	This signal is not used in this mode.	O	43
INPACK# (PC Card I/O Mode)	The Input Acknowledge signal is asserted when the card is selected and responds to an I/O read cycle at the address on the address bus.		
RFU (True IDE Mode)	In the True IDE mode, this signal is not used.		
IORD# (PC Card Memory Mode)	This signal is not used in this mode.	I	34
IORD# (PC Card I/O Mode)	This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the card when the card is configured to use the I/O interface.		
IORD# (True IDE Mode)	In the True IDE mode, the signal is the same as the		

Signal Name	Description	I/O	Pin
	I/O Mode.		

Signal Name	Description	I/O	Pin
IOWR# (PC Card Memory Mode)	This signal is not used in this mode	I	35
IOWR# (PC Card I/O Mode)	The I/O Write strobe is used to clock I/O data on the Data bus into the card controller registers when the card is configured to use the I/O interface.		
IOWR# (True IDE Mode)	In the True IDE Mode, this signal is the same as the I/O mode.		
RDY/BSY# (PC Card Memory Mode)	In the Memory Mode, this signal is set high when card is ready to accept a new data transfer operation and held low when the card is busy.	O	37
IREQ# (PC Card I/O Mode)	I/O Operation. After the card has been configured for I/O Mode, this signal is used as Interrupt Request.		
INTRQ (True IDE Mode)	In the True IDE Mode, this signal is the active high Interrupt Request to the host.		
WP (PC Card Memory Mode)	Memory Mode, the card doesn't have a write protect switch. This signal is held low.	O	24
IOIS16# (PC Card I/O Mode)	I/O Mode, A low signal indicates that a 16 bits or odd byte only operation can be performed by the addressed port.	-	-
IOCS16# (True IDE Mode)	In the True IDE Mode, this signal is asserted low when this device is expecting a word data transfer cycle.	-	-

7. CIS and Functions Configuration Registers

7.1 Card Information Structure (CIS)

The CIS is attribute information of the card and its characteristics, which includes information about the type of card and the manufacturer. The CIS is allocated in the beginning of the attribute memory, between addresses 0 and 255. The data is allocated in the even addresses only. The Host uses these registers to initialize and configure the card.

Addr.	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
000H	01H	CISTPL_JEDEC	Device info tuple	Tuple code
002H	03H	TPL_LINK	Link length is 3 byte	Link to next tuple
004H	D9H	Device Type W Speed	Type= D: I/O device WPS=1:No WP switch Speed=1: 250ns	Device type, WPS, speed
006H	01H	# address units-1 unit size	2 Kbytes of address space	Device size
008H	FFH	CISTPL_END	End of CISTPL_DEVICE	End marker
00AH	1CH	CISTPL_DEVICE_OC	Common memory other operating conditions tuple	Tuple code
00CH	04H	TPL_LINK	Link length is 4 byte	Link to next tuple
00EH	02H	Ext Reserved 3V M	3V=1:dual voltage card. Conditions for 3.3V operation M=0: conditions without wait	Other Conditions Information
010H	D9H	Device Type W Speed	Type=D:I/O device WPS=1:no WP switch Speed=1:250 ns	Device type, WPS, speed
012H	01H	#address units-1 unit size	2 Kbytes of address space	Device size
014H	FFH	CISTPL_END	End of CISTPL_DEVICE_OC	End marker
016H	18H	CISTPL_JEDEC_C	JEDEC programming info tuple	Tuple code
018H	02H	TPL_LINK	Link length is 2 byte	Link to next tuple
01AH	DFH	JEDEC ID	Device manufacturer ID	Manufacturer ID
01CH	01H	JEDEC Info	Manufacturer specific info	Manufacturer info
01EH	20H	CISTPL_MANFID	Manufacturer ID tuple	Tuple code
020H	20H	TPL_LINK	Link length is 4 bytes	Link to next tuple
022H	00H	TPLMID_MANF	PC Card manufacturer code	Manufacturer ID
024H	00H	TPLMID_MANF	PC Card manufacturer code	Manufacturer ID
026H	00H	TPLMID_CARD	Manufacturer specific info	Manufacturer info
028H	00H	TPLMID_CARD	Manufacturer specific info	Manufacturer info
02AH	21H	CISTPL_FUNCID	Function ID tuple	Tuple code
02CH	02H	CISTPL_LINK	Link length is 2 bytes	Link to next tuple
02EH	04H	TPLFID_FUNCTION	Fixed disk drive	Function code
030H	01H	Reserved R P	R=0: no expansion ROM P=1: configure at POST	System init byte TPLFID_SYSINIT
032H	22H	CISTPL_FUNCE	Function Extension tuple	Tuple code

Addr.	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
034H	02H	CISTPL_LINK	Link length is 2 bytes	Link to next tuple
036H	01H	Disk function extension tuple	Disk interface information	TPLFE_TYPE
038H	01H	Disk interface type	PC card ATA interface	TPLFE_DATA
03AH	22H	CISTPL_FUNCE	Function Extension tuple	Tuple code
03CH	03H	CISTPL_LINK	Link length is 3 bytes	Link to next tuple
03EH	02H	Disk function extension tuple	PC card ATA basic features	TPLFE_TYPE
040H	04H	Reserved D U S V	D=0:single drive on card U=0:no unique serial number S=1:silcon device V=0:no Vpp required	TPLFE_TYPE
042H	07H	R I E N P	I=0:twin IOIS16# unspecified E=0:index bit not emulated N=0:I/O includes 0x3F7 P=7:sleep,standy,idle supported	TPLFE_TYPE
044H	1AH	CISTPL_CONFIG	Configuration Tuple	Tuple code
046H	05H	TPL_LINK	Link length is 5 bytes	Link to next tuple
048H	01H	RFS RMS RAS	RFS:reserved RMS:1 byte register mask RAS:2 byte base address	Size of fields TPCC_SZ
04AH	07H	TPCC_LAST	Last configuration entry is 07H	Last entry index
04CH	00H	TPCC_RADR(LSB)	Configuration registers are located at 0200H	Configuration register location
04EH	02H	TPCC_RADR(MSB)	Configuration registers are located at 0200H	Configuration register location
050H	0FH	TPCC_RMSK	Configuration registers 0 to 3 are present	Configuration register present mask
052H	1BH	CISTPL_CFTABLE_ENTRY	Configuration tuple	Tuple code
054H	0BH	CISTPL_LINK	Link length is 11 bytes	Link to next tuple
056H	C0H	I D Configuration Index	Memory mapped configuration, Index=0 I=1:Interface byte follows D=1:Default entry	Configuration Table Index Byte TPCE_INDX
058H	C0H	W R P B Interface type	W=1: wait required R=1: ready/busy active P=0: WP not used B=0: BVD1,BVD2 not used Type=0: Memory interface	Interface Description TPCE_IF
05AH	A1H	M MS IR IO T Power	M=1: misc info present MS=1: 2 byte memory length IR=0: no interrupt is used IO=0: no I/O space is used T=0: no timing info specified Power=1: Vcc info, no Vpp	Feature Selection Byte TPCE_FS
05CH	27H	R DI PI AI SI HV LV NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	Power Description Structure Parameter Selection Byte TPCE_PD
05EH	55H	X Mantissa Exponent	Nominal voltage 5.0V	-
060H	4DH	X Mantissa Exponent	Minimum voltage 4.5V	-
062H	5DH	X Mantissa Exponent	Maximum voltage 5.5V	-
064H	75H	X Mantissa Exponent	Peak current 80mA	-
066H	08H	Length in 256 byte	Length of memory space is 2	Memory space

Addr.	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
		units(LSB)	kbytes	Descr. TPCE_MS
068H	00H	Length in 256 byte units(MSB)	Length of memory space is 2 kbytes	Memory space Desr. TPCE_MS
06AH	21H	X R P RO A T	X=0: no more misc fields P=1: power-down supported RO=0: read/write media A=0: audio not supported T=1: max twins is 1	Miscellaneous Features TPCE_MI
06CH	1BH	CISTPL_CFTABLE_ENTRY	Configuration tuple	Tuple code
06EH	06H	CISTPL_LINK	Link length is 6 bytes	Link to next tuple
070H	00H	I D Configuration Index	Memory mapped configuration, index=0	TPCE_INDX
072H	01H	M MS IR IO T Power	Power=1: Vcc info, no Vpp	TPCE_FS
074H	21H	R DI PI AI SI HV LV NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
076H	B5H	X Mantissa Exponent	X=1: extension byte present	-
078H	1EH	X Extension	Nominal voltage 3.30V	-
07AH	4DH	X Mantissa Exponent	Peak current 45mA	-
07CH	1BH	CISTPL_CFTABLE_ENTRY	Configuration tuple	Tuple code
07EH	0DH	CISTPL_LINK	Link length is 13 bytes	Link to next tuple
080H	C1H	I D Configuration Index	I/O mapped, index=1 I=1: Interface byte follows D=1: Default entry	TPCE_INDEX
082H	41H	W R P B Interface type	W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O Interface	TPCE_IF
084H	99H	M MS IR IO T Power	M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: Vcc info, no Vpp	TPCE_FS
086H	27H	R DI PI AI SI HV LV NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
088H	55H	X Mantissa Exponent	Nominal voltage 5.0V	-
08AH	4DH	X Mantissa Exponent	Minimum voltage 4.5V	-
08CH	5DH	X Mantissa Exponent	Maximum voltage 5.5V	-
08EH	75H	X Mantissa Exponent	Peak current 80mA	-
090H	64H	R S E IO	S=1: support 16 bit hosts E=1: support 8 bit hosts IO=4: 4 address lines decoded	TPCE_IO

Addr.	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
092H	B0H	S P L M V B I N	S=1: interrupt sharing logic P=0: pulse mode not supported L=1: level mode supported M=1: masks V..N present V=0: no vendor unique IRQ B=0: no bus error IRQ I=0: no I/O check IRQ N=0: no NMI	TPCE_IR
094H	FFH	IRQ7..0	Interrupt signal may be assigned to any host	-
096H	FFH	IRQ15..8	Interrupt signal may be assigned to any host	-
098H	21H	X R P RO A T	X=0: no more misc fields P=1: power-dowm supported RO=0: read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
09AH	1BH	CISTPL_CFTABLE_ENTRY	Configuration tuple	Tuple code
09CH	06H	CISTPL_LINK	Link length is 6 bytes	Link to next tuple
09EH	01H	I D Configuration Index	I/O mapped, index=1	TPCE_INDX
0A0H	01H	M MS IR IO T Power	Power=1: Vcc info, no Vpp	TPCE_FS
0A2H	21H	R DI PI AI SI HV LV NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
0A4H	B5H	X Mantissa Exponent	X=1: extension byte present	-
0A6H	1EH	X Extension	Nominal voltage 3.30V	-
0A8H	4DH	X Mantissa Exponent	Peak current 45mA	-
0AAH	1BH	CISTPL_CFTABLE_ENTRY	Configuration tuple	Tuple code
0ACH	12H	CISTPL_LINK	Link Length is 18 bytes	Link to next tuple
0AEH	C2H	I D Configuration Index	I/O mapped, index=2 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
0B0H	41H	W R P B Interface type	W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1,BVD2 not used Type=1: I/O Interface	TPCE_IF
0B2H	99H	M MS IR IO T Power	M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: Vcc info,no Vpp	TPCE_FS
0B4H	27H	R DI PI AI SI HV LV NV	DI: no power-down current PI=1: peak current info AI: no average current info	TPCE_PD

Addr.	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
			SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	
0B6H	55H	X Mantissa Exponent	Nominal voltage 5.0V	-
0B8H	4DH	X Mantissa Exponent	Minimum voltage 4.5V	-
0BAH	5DH	X Mantissa Exponent	Maximum voltage 5.5V	-
0BCH	55H	X Mantissa Exponent	Peak current 80 mA	-
0BEH	EAH	R S E IO	R=1: range follows S=1: support 16 bit hosts E=1: support 8 bit hosts IO=10: 10 lines decoded	TPCE_IO
0C0H	61H	LS AS NR	LS=1: 1 byte length AS=2: 2 byte address NR=1: 2 address ranges	-
0C2H	F0H	Base address 1(LSB)	Address range 1 0x1F0 to 0x1F7	-
0C4H	01H	Base address 1(MSB)	Address range 1 0x1F0 to 0x1F7	-
0C6H	07H	Address range 1 length	Address range 1 0x1F0 to 0x1F7	-
0C8H	F6H	Base address 2(LSB)	Address range 2 0x3F6 to 0x3F7	-
0CAH	03H	Base address 2(MSB)	Address range 2 0x3F6 to 0x3F7	-
0CCH	01H	Address range 2 length	Address range 2 0x3F6 to 0x3f7	-
0CEH	AEH	S P L M IRQN	S=1: interrupt sharing logic P=0: pulse mode not supported L=1: level mode supported M=0: masks V..N not present IRQN=14: use interrupt 14	TPCE_IR
0D0H	21H	X R P RO A T	X=0: no more misc fields P=1: power-down supported RO=0: read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI
0D2H	1BH	CISTPL_CFTABLE_ENTRY	Configuration tuple	Tuple code
0D4H	06H	CISTPL_LINK	Link length is 6 bytes	Link to next tuple
0D6H	02H	I D Configuration Index	I/O mapped, index=2	TPCE_INDX
0D8H	01H	M MS IR IO T Power	Power=1: Vcc info, no Vpp	TPCE_FS
0DAH	21H	R DI PI AI SI HV LV NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
0DCH	B5H	X Mantissa Exponent	X=1: extension byte present	-
0DEH	1EH	X Extension	Nominal voltage 3.30V	-
0E0H	4DH	X Mantissa Exponent	Peak current 45mA	-
0E2H	1BH	CISTPL_CFTABLE_ENTRY	Configuration tuple	Tuple code
0E4H	12H	CISTPL_LINK	Link length is 18 bytes	Link to next tuple

Addr.	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0E6H	C3H	I D Configuration Index	I/O mapped, index=3 I=1: Interface byte follows D=1: Default entry	TPCE_INDX
0E8H	41H	W R P B Interface type	W=0: wait not required R=1: ready/busy active P=0: WP not used B=0: BVD1, BVD2 not used Type=1: I/O interface	TPCE_IF
0EAH	99H	M MS IR IO T Power	M=1: misc info present MS=0: no memory space info IR=1: interrupt is used IO=1: I/O space is used T=0: no timing info specified Power=1: Vcc info, no Vpp	TPCE_FS
0ECH	27H	R DI PI AI SI HV LV NV	DI: no power-down current PI=1: peak current info AI: no average current info SI: no static current info HV=1: max voltage info LV=1: min voltage info NV=1: nominal voltage info	TPCE_PD
0EEH	55H	X Mantissa Exponent	Nominal voltage 5.0V	-
0F0H	4DH	X Mantissa Exponent	Minimum voltage 4.5V	-
0F2H	5DH	X Mantissa Exponent	Maximum voltage 5.5V	-
0F4H	75H	X Mantissa Exponent	Peak current 80mA	-
0F6H	EAH	R S E IO	R=1: range follows S=1: support 16 bit hosts E=1: support 8 bit hosts IO=10: 10 lines decoded	TPCE_IO
0F8H	61H	LS AS NR	LS=1: 1byte length AS=2: 2byte address NR=1: 2 address ranges	-
0FAH	70H	Base address 1 (LSB)	Address range 1 0x170 to 0x177	-
0FEH	01H	Base address 1 (MSB)	Address range 1 0x170 to 0x177	-
0FCH	07H	Address range 1 length	Address range 1 0x170 to 0x177	-
100H	76H	Base address 2(LSB)	Address range 2 0x376 to 0x377	-
102H	03H	Base address 2(MSB)	Address range 2 0x376 to 0x377	-
104H	01H	Address range 2 length	Address range 2 0x376 to ox377	-
106H	AEH	S P L M IRQN	S=1: interrupt sharing logic P=0: pulse mode not supported L=1: level mode supported M=0: masks V..N not present IRQN=14: use interrupt 14	TPCE_IR
108H	21H	X R P RO A T	X=0: no more misc fields P=1: power-down supported RO=0: read/write media A=0: audio not supported T=1: max twins is 1	TPCE_MI

Addr.	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
10AH	1BH	CISTPL_CFTABLE_ENTRY	Comfiguration tuple	Tuple code
10CH	06H	CISTPL_LINK	Link length is 6 bytes	Link to next tuple
10EH	03H	I D Configuration Index	I/O mapped, index=3	TPCE_INDX
110H	01H	M MS IR IO T Power	Power=1: Vcc info, no Vpp	TPCE_FS
112H	21H	R DI PI AI SI HV LV NV	PI=1: peak current info NV=1: nominal voltage info	TPCE_PD
114H	B5H	X Mantissa Exponent	X=1: extension byte present	-
116H	1EH	X Extension	Nominal voltage 3.30V	-
118H	4DH	X Mantissa Exponent	Peak current 45mA	-
11AH	1BH	CISTPL_CFTABLE_ENTRY	Configuration tuple	Tuple code
11CH	04H	CISTPL_LINK	Link length is 4 bytes	Link to next tuple
11EH	07H	I D Configuration Index	I/O mapped, index=7	TPCE_INDX
120H	00H	M MS IR IO T Power	No feature descriptions	TPCE_FS
122H	28H	-	Reserved	-
124H	D3H	-	Reserved	-
126H	14H	CISTPL_NO_LINK	No link control tuple	Tuple code
128H	00H	CISTPL_LINK	Link length is 0 bytes	Link to next tuple
12AH	15H	CISTPL_VERS_1	Level 1 version/product info	Tuple code
12CH	15H	CISTPL_LINK	Link length is 21 bytes	Link to next tuple
12EH	04H	TPPLV1_MAJOR	PCMCIA2.0/JEIDA4.1	Major version
130H	01H	TPPLV1_MINOR	PCMCIA2.0/JEIDA4.1	Minor Version
132H	48H	-	Reserved	-
146H	00H	-	Null terminator	-
148H	4DH		Model 1	-
154H	00H		Null terminator	-
156H	FFH	CISTPL_END	End of CISTPL_VERS_1	End marker
158H	FFH	CISTPL_END	End of CIS	Tuple code

7.2 Identify Device Information

Identify Device ATA command in the True-IDE mode

Word address	Default value	Bytes	Data field type information
0	045AH	2	General configuration bit-significant information (-id2)
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	0200H	2	Number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7 to 8	XXXXH	4	Number of sectors per card
9	0000H	2	Reserved
10 to 19	XXXXH	20	Serial Number (20 ASCII characters)
20	0002H	2	Buffer type (dual-ported multi-sector)
21	0001H	2	Buffer size in 512 byte increments
22	0004H	2	# ECC bytes passed on Read/Write Long Commands
23 to 26	XXXXH	8	Firmware revision (8 ASCII characters)
27 to 46	XXXXH	40	Model Number (40 ASCII characters)
47	8001H	2	Maximum 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0F00H	2	Capabilities: DMA, LBA, IORDY supported
50	4001H	2	Capabilities: device specific standby timer minimum
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	DMA data transfer cycle timing mode not supported
53	0007H	2	Data Fields 54 to 58, 64 to 70 and 88 are valid
54	XXXXH	2	Number of current logical cylinders
55	XXXXH	2	Number of current logical heads
56	XXXXH	2	Number of current logical sectors per track
57 to 58	XXXXH	4	Current Capacity in sectors
59	010XH	2	Multiple sector setting is valid
60 to 61	XXXXH	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Single Word DMA transfer not implemented
63	0X0XH	2	Multi Word DMA transfer mode, mdma preformat option
64	0003H	2	Advanced PIO Modes: modes 3 and 4 supported
65	0078H	2	Minimum Multi Word DMA cycle time, 0 if no MDMA

66	0078H	2	Recommended Multi Word DMA cycle time, 0 if no MDMA
67	0078H	2	Minimum PIO cycle time without flow control
68	0078H	2	Minimum PIO cycle time with flow control
69 to 79	0000H	22	Reserved
80	0020H	2	Major version number, ATA-5 support
81	0000H	2	Minor version number, not reported
82	740BH	2	Command set: NOP, READ BUFFER, WRITE BUFFER, host protected area, power management feature set, Security Mode feature set, SMART feature set
83	5005H	2	Command set: FLUSH CACHE, CFA feature set, DOWNLOAD MICROCODE
84	4000H	2	Command set/feature supported extension
85	740XH	2	Command set enabled: NOP, READ BUFFER, WRITE BUFFER, host protected area, power management feature set, Security Mode feature set enabled/disabled, SMART feature set enabled/disabled
86	1005H	2	Command set enabled: FLUSH CACHE, CFA feature set, DOWNLOAD MICROCODE
87	4000H	2	Command set/feature default
88	XXXXH	2	UDMA mode, according to udma preformat option
89	0000H	2	Time for Security Erase Unit not specified
90	0000H	2	Time for Enhanced Security Erase Unit not specified
91	0000H	2	Reserved
92	XXXXH	2	Master Password Revision Code
93	XXXXH	2	Hardware Reset Result
94 to 127	0000H	72	Reserved
128	0XXXH	2	Security Status
129	XX00H	2	Write Protect Status. Bit 15 = permanent write protect, no more spare blocks available, Bit 14 = permanent write protect due to internal table corruption
130 to 133	XXXXH	8	Firmware date string
134	848AH	2	General Configuration word for PCMCIA mode (-id1)
135	045AH	2	General Configuration word for True-IDE mode (-id2)
136 to 141	XXXXH	12	Firmware file name
142 to 147	XXXXH	12	Preformat file name
148 to 153	XXXXH	12	Anchor program file name
154 to 159	0000H	12	Reserved

160	A064H	2	CFA Power Mode: no power level 1, max 100mA
161	0000H	2	Reserved
162	0000H	2	Key Management Schemes: CPRM not supported
163	XXXXH	2	CFA advanced modes: supported and enabled bits
164	001BH	2	CFA advanced modes: 80ns I/O and Memory supported
165 to 254	0000H	180	Reserved
255	XXA5H	2	Integrity Word

In PCMCIA mode,the following words will be different

Word address	Default value	Bytes	Data field type information
0	848AH	2	General configuration bit-significant information (-id1)
49	0E00H	2	Capabilities: LBA, IORDY supported
63	0000H	2	Multi Word DMA transfer mode not supported
65	0000H	2	Minimum Multi Word DMA cycle time
66	0000H	2	Recommended Multi Word DMA cycle time
93	0000H	2	Hardware Reset Result not supported

8. ATA COMMAND

8.1 ATA Protocol Overview

Command classes are grouped according to protocols described for command execution. For all commands, the host must first check for BYS=0 before proceeding further. For most commands, the host should not proceed until DRDY=1.

8.1.1 PIO Data In Commands

Execution includes one more 512 bytes data-sector drive-to-host transfer. If the drive presents error status, it prepares to transfer data at the host's discretion. The host writes parameters to the Feature, Sector Count, Sector Number, Cylinder, and Drive/Head register. The host writes the Command Register's command code. The drive sets BSY and prepares for data transfer when a data sector is available; the drive sets DRQ, clears BSY, and asserts interrupt. At interrupt, the host reads the Status register, the drive negates interrupt, and the host reads one data-sector from Data Register. The drive clears DRQ. If another sector is required, the drive sets BSY and repeats the data transfer.

8.1.2 PIO Data Out Commands

Execution includes one or more 512 bytes host-to-drive data-sector transfers. The host writes parameters to the Features, Sector Count, Sector Number, Cylinder, and

Drive/Head Registers. The host writes the Command register's command code. The drive sets DRQ when it can accept the first sector of data

The host writes one sector of data to the Data register. The Drive clears DRQ and sets BSY. At sector processing complete, the drive clears BSY and asserts interrupt. If another sector transfer is required, the drive also sets DRQ. The host reads the Status register after detecting interrupt. The drive negates the interrupt if another sector transfer is required, the sequence repeats the data transfer.

8.1.3 Non Data Commands

Command execution involves no data transfer. The host writes parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head registers. The host writes the Command register's command code. The Drive sets BSY. When the drive completes sector processing, it clears BSY and asserts interrupt. The host reads the Status register after detecting interrupts the drive negates the interrupt.

8.2 Supported ATA Commands

No.	Command name	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check power mode	E5H, 98H	-	-	-	-	Y	-	-
2	Download Microcode	92H	Y	Y	Y	-	Y	-	-
3	Erase sector(s)	C0H	-	Y	Y	Y	Y	Y	Y
4	Execute drive diagnostic	90H	-	-	-	-	-	-	-
5	Flush Cache	E7H	-	-	-	-	Y	-	-
6	Format track	50H	-	Y	-	Y	Y	Y	Y
7	Identify Device	ECH	-	-	-	-	Y	-	-
8	Idle	E3H, 97H	-	Y	-	-	Y	Y	-
9	Idle immediate	E1H, 95H	-	-	-	-	Y	-	-
10	Initialize drive parameters	91H	-	Y	-	-	Y	Y	-
11	Media Lock	DEH	-	-	-	-	Y	-	-
12	Media Unlock	DEH	-	-	-	-	Y	-	-
13	NOP	00H	-	-	-	-	Y	-	-
14	Read buffer	E4H	-	-	-	-	Y	-	-
15	Read DMA	C8H, C9H	-	Y	Y	Y	Y	Y	Y
16	Read multiple	C4H	-	Y	Y	Y	Y	Y	Y
17	Read long	22H, 23H	-	-	Y	Y	Y	Y	Y
18	Read native max address	F8H	-	-	-	-	Y	-	-
19	Read sector(s)	20H, 21H	-	Y	Y	Y	Y	Y	Y
20	Read verify sector(s)	40H, 41H	-	Y	Y	Y	Y	Y	Y

21	Recalibrate	1XH	-	-	-	-	Y	-	-
22	Request sense	03H	-	-	-	-	Y	-	-
23	Security Disable Password	F6H	-	-	-	-	Y	-	-
24	Security Erase Prepare	F3H	-	-	-	-	Y	-	-
25	Security Erase Unit	F4H	-	-	-	-	Y	-	-
26	Security Freeze Lock	F5H	-	-	-	-	Y	-	-
27	Security Set Password	F1H	-	-	-	-	Y	-	-
28	Security Unlock	F2H	-	-	-	-	Y	Y	-
29	Seek	7XH	-	-	Y	Y	Y	Y	Y
30	Set features	EFH	Y	-	-	-	Y	-	-
31	Set max address	F9H	-	Y	Y	Y	Y	Y	Y
32	Set multiple mode	C6H	-	Y	-	-	Y	-	-
33	Set sleep mode	E6H, 99H	-	-	-	-	Y	-	-
34	SMART	B0H	Y	Y	-	Y	Y	-	-
35	Stand by	E2H, 96H	-	Y	-	-	Y	-	-
36	Stand by immediate	E0H, 94H	-	-	-	-	Y	-	-
37	Translate sector	87H	-	Y	Y	Y	Y	Y	Y
38	Write buffer	E8H	-	-	-	-	Y	-	-
39	Write DMA	CAH, CBH	-	Y	Y	Y	Y	Y	Y
40	Write long	32H, 33H	-	-	Y	Y	Y	Y	Y
41	Write multiple	C5H	-	Y	Y	Y	Y	Y	Y
42	Write multiple w/o erase	CDH	-	Y	Y	Y	Y	Y	Y
43	Write sector(s)	30H, 31H	-	Y	Y	Y	Y	Y	Y
44	Write sector(s) w/o erase	38H	-	Y	Y	Y	Y	Y	Y
45	Write verify	3CH	-	Y	Y	Y	Y	Y	Y

Notes: FR: Feature Register

SC: Sector Count register(00H to FFH,00H means 256 sectors)

SN: Sector Number register

CY: Cylinder Low/High register

DR: Drive bit of Drive/Head register

HD: Head No.(0 to 15) of Drive/Head register

Y: Used for the command

-: Not used for the command

Check power mode

PROTOCOL - Non-data command.

The Sector Count register is set to 0 (00h) if the device is in Standby mode, and to 255

(FFh) if the device is in Active mode.

Download Microcode

PROTOCOL - PIO data in.
This command is used to update the firmware on the device. A 16 bit sector count is transferred in the Sector Count (lower 8 bits) and Sector Number (higher 8 bits) registers. If this sector count is 0, then the firmware area is refreshed with no change to the firmware. No data is transferred in this case. If the sector count is non-zero, it must be 129, and this many sectors must be sent to the card. The first sector is the new anchor file, the following 128 sectors are the new firmware file. The Feature Register must be 7. The new firmware is installed on the card, and is activated at the next power-on. The card configuration stays unchanged, except for Identify Device words 130 to 133, these show the new firmware version information.
The Download Microcode command fails if the new firmware is not compatible to the currently installed firmware.

Erase sector(s)

PROTOCOL - Non-data command.
This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command.

Execute drive diagnostic

PROTOCOL - Non-data command.
This command performs the internal diagnostic tests of the device. The test result is written to the Error register. The Dev bit in the Device/Head register is ignored for this command.

Execute drive diagnostic

PROTOCOL - Non-data command.
This command performs the internal diagnostic tests of the device. The test result is written to the Error register. The Dev bit in the Device/Head register is ignored for this command.

Flush cache

PROTOCOL - Non-data command.
This command flushes all unwritten data to the flash.

Format track

PROTOCOL - PIO data out.

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h).

Identify Device

PROTOCOL - PIO data in.
This command sets up the device‟s parameter information (256 words) as specified in section 4.3 in the sector buffer.

Idle, Idle immediate

PROTOCOL - Non-data command.
This command causes the device to enter the Idle Mode.

Initialize drive parameters

PROTOCOL - Non-data command.
This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1, per logical cylinder for the current CHS translation mode.

Media Lock, Media Unlock

PROTOCOL – Non-data command.
There is no lock or unlock functionality, these commands act as a no operation.

NOP

PROTOCOL – Non-data command.
This command always fails with an aborted command error.

Read buffer

PROTOCOL - PIO data in.
This command enables the host to read the current contents of the device‟s sector buffer.

Read DMA

PROTOCOL - DMA data in.
This command reads from 1 to 256 sectors as specified in the Sector Count register. The transfer begins at the specified LBA or CHS address.

Read multiple

PROTOCOL - PIO data in.

This command is identical to the Read Sector(s) command except that interrupts may be generated every sector or every second sector.

Read native max address

PROTOCOL - Non-data command.
The native maximum address (highest address accepted in the factory default condition) is returned.

Read long

PROTOCOL - PIO data in.
This command performs similarly to the Read Sector(s) command except that it returns the data and a number of vendor specific bytes appended to the data field of the desired sector. Only single sector Read Long operations are supported.

Read sector(s)

PROTOCOL - PIO data in.
This command performs similarly to the Read Sector(s) command except that it returns the data and a number of vendor specific bytes appended to the data field of the desired sector. Only single sector Read Long operations are supported.

Read sector(s)

PROTOCOL - PIO data in.
This command reads from 1 to 256 sectors as specified in the Sector Count register. The transfer begins at the specified LBA or CHS address.

Read verify sector(s)

PROTOCOL - Non-data command.
This command is identical to the Read Sector(s) command, except that the DRQ bit is never set, and no data is transferred to the host. The functionality of this command can be selected.

Recalibrate

PROTOCOL - Non-data command.
This command is effectively a NOP command and is provided for compatibility purposes.

Request sense

PROTOCOL - Non-data command.

This command requests extended error information for the previous command. The extended error code is returned to the host in the Error Register.

Security Disable Password

PROTOCOL - PIO data out.
This command checks and removes the Security Mode password.

Security Erase Prepare

PROTOCOL - Non-data command.
This command prepares for a Security Erase Unit command.

Security Erase Unit

PROTOCOL - PIO data out.
This command checks the Security Mode password and erases the whole device.

Security Freeze Lock

PROTOCOL - Non-data command.
This command disables further Security Mode commands until the next hardware reset or power on.

Security Set Password

PROTOCOL - PIO data out.
This command sets the Security Mode password.

Security Unlock

PROTOCOL - PIO data out.
This command enables access to a locked device.

Seek

PROTOCOL - Non-data command.
This command is effectively a NOP command although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

Set features

PROTOCOL - Non-data command.
This command is used by the host to establish parameters which affect the execution of

certain device features. The following features are supported:

Value	Command	Value	Command
01h/81h	Enable/disable 8-bit data transfers	02h/82h	Enable/disable write cache
03h	Set transfer mode	05h/85h	Enable/disable advanced power management
09h/89h	Enable/disable extended power operations	0Ah/8Ah	Enable/disable power level 1 commands
55h/AAh	Disable/enable Read Look Ahead.	66h/CCh	Disable/enable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.	96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility.	9Ah	Set the host current source capability.
BBh	4 bytes of data apply on Read/Write Long commands.		

Set max address

PROTOCOL - Non-data command.

This command sets a temporary or permanent new maximum address.

Set multiple mode

PROTOCOL - Non-data command.

This command establishes the block count for Read Multiple and Write Multiple commands. Depending on the configuration, values of 1 or 2 are supported.

Set sleep mode

PROTOCOL - Non-data command.

This command causes the device to enter Sleep Mode.

SMART

PROTOCOL - Non-data or PIO data in.

This command implements the ATA S.M.A.R.T. functionality.

Stand by, Stand by immediate

PROTOCOL - Non-data command.

This command causes the device to enter the Standby Mode.

Translate sector

PROTOCOL - Non-data command.
This command is effectively a no operation command and only implemented for backward compatibility. The Sector Count Register will always be returned with 00h.

Wear level

PROTOCOL - Non-data command.
This command is effectively a no operation command and only implemented for backward compatibility. The Sector Count Register will always be returned with 00h.

Write buffer

PROTOCOL - PIO data out.
This command enables the host to overwrite the contents of the device‟s sector buffer.

Write DMA

PROTOCOL - DMA data out.
This command writes from 1 to 256 sectors as specified in the Sector Count register. The transfer begins at the specified LBA or CHS address.

Write long

PROTOCOL - PIO data out.
This command is similar to the Write Sector(s) command except that it writes the data and the vendor specific bytes as supplied by the host; the device does not generate the vendor specific bytes itself.
Only single sector Write Long operations are supported.

Write multiple

PROTOCOL - PIO data out.
This command is identical to the Write Sector(s) except that interrupts may be generated every sector or every second sector.

Write multiple w/o erase

PROTOCOL - PIO data out.
This command is identical to the Write Multiple command.

Write sector(s)

PROTOCOL - PIO data out.
This command writes from 1 to 256 sectors as specified in the Sector Count register. The

transfer begins at the specified LBA or CHS address.

Write sector(s) w/o erase

PROTOCOL - PIO data out.

This command is identical to the Write Sector(s) command.

Write verify

PROTOCOL - PIO data out.

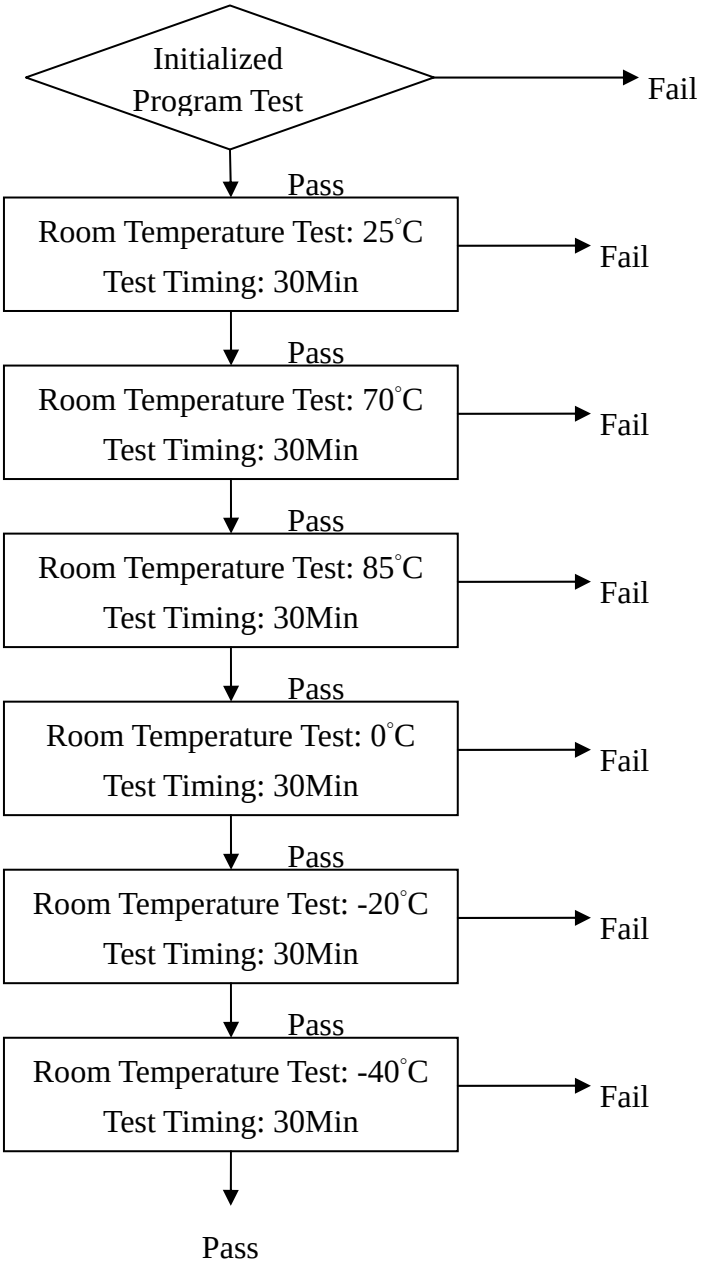
This command is similar to the Write Sector(s) command except that each sector is verified before the command is completed.

8.3 S.M.A.R.T. Functionality

Value	Command
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute Autosave
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
E0h	SMART Read Remap Data
E1h	SMART Read Wear Level Data

9. System Environmental Specifications

9.1 Temperature Test Flow



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