7. ATA & TRUE IDE REGISTER DECODING

SiliconDrive PC can be configured as either Memory Mapped or I/O Devices. As noted earlier communication to and from the SiliconDrive is accomplished using the ATA Command Block.

7.1. Memory Mapped Register Decoding

In Memory Mapped mode, the SiliconDrives registers are accessed via standard memory references (i.e., OE# and WE#). The ATA registers are mapped to common memory space in a 2K byte window starting at address 0.

Reg#	Offset	A10	A9:A4	A3	A2	A1	A0	OE# = L	WE# = L
1	0	0	X	0	0	0	0	Even Data Read	Even Data Write
1	1	0	X	0	0	0	1	Error	Feature
1	2	0	X	0	0	1	0	Sector Count	Sector Count
1	3	0	X	0	0	1	1	Sector Number	Sector Number
1	4	0	X	0	1	0	0	Cylinder Low	Cylinder Low
1	5	0	X	0	1	0	1	Cylinder High	Cylinder High
1	6	0	X	0	1	1	0	Drive/Head	Drive/Head
1	7	0	X	0	1	1	1	Status	Command
1	8	0	X	1	0	0	0	Duplicate Even Data Read	Duplicate Even Data Write
1	9	0	X	1	0	0	1	Duplicate Odd Data Read	Duplicate Odd Data Write
1	D	0	X	1	1	0	1	Duplicate Error	Duplicate Feature
1	E	0	X	1	1	1	0	Alternate Status	Device Control
1	F	0	X	1	1	1	1	Drive Address	Reserved
1	X	1	X	X	X	X	0	Even Data Read	Even Data Write
1	X	1	X	X	X	X	1	Odd Data Read	Odd Data Write

7.2. Independent I/O Mode Register Decoding

Independent I/O Mode, or Contiguous I/O mode requires the host to decode a contiguous block of 16 I/O registers to select the SiliconDrive PC.

REG#	Offset	A10	A9:A4	A3	A2	A1	A0	IORD# = L	IOWR# = L
0	0	X	X	0	0	0	0	Even Data Read	Even Data Write
0	1	X	X	0	0	0	1	Error	Feature
0	2	X	X	0	0	1	0	Sector Count	Sector Count
0	3	X	X	0	0	1	1	Sector Number	Sector Number
0	4	X	X	0	1	0	0	Cylinder Low	Cylinder Low
0	5	X	X	0	1	0	1	Cylinder High	Cylinder High
0	6	X	X	0	1	1	0	Drive/Head	Drive/Head
0	7	X	X	0	1	1	1	Status	Command
0	8	X	X	1	0	0	0	Duplicate Even Data Read	Duplicate Even Data Write
0	9	X	X	1	0	0	1	Duplicate Odd Data Read	Duplicate Odd Data Write
0	D	X	X	1	1	0	1	Duplicate Error	Duplicate Feature
0	E	X	X	1	1	1	0	Alternate Status	Device Control
0	F	X	X	1	1	1	1	Drive Address	Reserved

7.3. Primary and Secondary I/O Mapped Register Decoding

REG#	A10	A9:A4 Primary	A9:A4 Secondary	A3	A2	A1	A0	IORD# = L	IOWR# = L
0	X	1Fxh	17xh	0	0	0	0	Even Data Read	Even Data Write
0	X	1Fxh	17xh	0	0	0	1	Error	Feature
0	X	1Fxh	17xh	0	0	1	0	Sector Count	Sector Count
0	X	1Fxh	17xh	0	0	1	1	Sector Number	Sector Number
0	X	1Fxh	17xh	0	1	0	0	Cylinder Low	Cylinder Low
0	X	1Fxh	17xh	0	1	0	1	Cylinder High	Cylinder High
0	X	1Fxh	17xh	0	1	1	0	Drive/Head	Drive/Head
0	X	1Fxh	17xh	0	1	1	1	Status	Command
0	X	3Fxh	37xh	0	1	1	0	Alternate Status	Device Control
0	X	3Fxh	37xh	0	1	1	1	Drive Address	Reserved

7.4. Task File Register Specification

The Task File Registers are used for reading and writing the storage data in the SiliconDrive PC. The decoded addresses are as shown.

CS0#	CS1#	DA02	DA01	DA00	DIOR# = L	DIOW# = L
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	0	1	1	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command
0	0	X	X	X	Invalid	Invalid
1	1	X	X	X	High-Z	Not Used
1	0	0	X	X	High-Z	Not Used
1	0	1	0	X	High-Z	Not Used
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used

8. ATA REGISTERS

8.1. Data Register

The Data Register is a 16-bit Register used to transfer data blocks between the Host and the Drive buffer. This register may set to 8-bit mode by using the Set Features Command defined in Section 9.1.15.

8.2. Error Register

The Error Register contains the error status, if any, generated from the last executed ATA Command. The contents are qualified by the ERR bit being set in the Status Register Section 8.9.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read	BBK	UNC	MC	IDNF	MCR	ABRT	TKNOF	AMNF
Default Value	0	0	0	0	0	0	0	0

Notes

Bit 7: BBK (Bad Block Detected)	Set when a Bad Block is detected.
Bit 6: UNC (Uncorrectable Data Error)	Set when Uncorrectable Error is encountered.
Bit 5: MC (Media Changed)	Set to 0.
Bit 4: IDNF (ID Not Found)	Set when Sector ID not found.
Bit 3: MCR (Media Change Request)	Set to 0.
Bit 2: ABRT (Aborted Command)	Set when Command Aborted due to drive error.
Bit 1: TKONF (Track 0 Not Found)	Set when Executive Drive Diagnostic Command. Bit
0: AMNF (Address mark Not Found)	Set in case of a general error.

8.3. Feature Register

The Feature Register is command specific and is used to enable and disable interface features. This register supports either odd or even byte data transfers only.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Feature Byte							

8.4. Sector Count Register

The Sector Count Register is used to read or write the sector count of the data for which an ATA transfer has been made.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Sector Count							
Default Value	0	0	0	0	0	0	0	1

8.5. Sector Number Register

The Sector Number Register is set by the host to specify the starting sector number associated with the next ATA command to be executed. Following a qualified ATA command sequence the device will set the register value to the last sector read or written as a result of the previous AT command.

When LBA mode is implemented and the host issues a command the contents of this register describe the Logical Block Number bits A[7:0]. Following an ATA Command the device will load this register with the LBA block number resulting from the last ATA command.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Sector Number (CHS Addressing)							
	Logical Block Number bits A07-A00 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	1

8.6. Cylinder Low Register

The Cylinder Low Register is set by the host to specify the cylinder number low byte. Following an ATA command, the contents of this register is written by the device, identifying the cylinder number low byte.

In LBA mode, this 8-bit register maintains the contents of the Logical Block number address bits A15:A08.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A15-A08 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

8.7. Cylinder High Register

The Cylinder High Register is set by the host to specify the cylinder number high byte. Following an ATA command, the contents of this register is set internally by the device, identifying the cylinder number high byte.

In LBA mode, this 8-bit register maintains the contents of the Logical Block number address bits A23:A16.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A23-A16 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

8.8. Drive/Head Register

The Drive/Head Register is used by the host and the device to select the type of addressing (CHS or LBA), the drive letter, and either bits 3 through 0 of the head number is CHS mode or in LBA mode bits D3:D0 reflect the logical block number bits LBA27:LBA24.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	1	LBA	1	DRV	HS3 LBA27	HS2 LBA26	HS1 LBA25	HS0 LBA24
Default Value	1	0	1	0	0	0	0	0

The Drive/Head Register is used by the host, to specify one of a pair of ATA drives present in the platform.

Notes

Bit 6: LBA (Logical Block Addressing)	Selects between CHS (0) and LBA (1) addressing mode.
Bit 4: DRV (Drive Address) Bits 3 - 0: HS3 to 0 mode.	Indicates the drive number selected by the host, either 0 or 1. Indicates bits 3 to 0 of the head number in CHS addressing or LBA bits 27 thru 24 in LBA mode.
CHS to LBA conversion:	LBA = (C x Hpc + H) x SpH + S –1
LBA to CHS conversion:	C = LBA / (HpC x SpH) H = (LBA / SpH) mod (HpC) S = (LBA mod(SpH)) + 1
Where:	'C' is the Cylinder Number. 'H' is the Head Number. 'S' is the Sector Count. 'HpC' is the Head count per Cylinder Count. 'SpH' is the Sector count per Head Count (Track).

8.9. Status Register

The Status Register provides the device's current status to the host. The status register is an 8-bit read only register. When the contents of this register are read by the host, the IREQ# bit is cleared.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

Notes

Bit 7: BSY (Busy)	Set when the drive is busy and unable to process any new ATA commands.
Bit 6: DRDY (Data Ready)	Set when the device is ready to accept ATA commands from the host.
Bit 5: DWF (Drive Write Fault)	Always set to 0.
Bit 4: DSC (Drive Seek Complete)	Set when the drive heads have been positioned over a specific track.
Bit 3: DRQ (Data Request)	Set when device is read to transfer a word or byte of data to or from the host and the device.
Bit 2: CORR (Corrected Data)	Always set to 0.
Bit 1: IDX (Index)	Always set to 0.
Bit 0: ERR (Error)	Set when an error occurred during the previous ATA command.

8.10. Command Register

The Command Register specifies the ATA Command code being issued to the drive by the host. Execution of the command begins immediately following the issuance of the command register code by the host.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	ATA Command Code							

Refer to Section 9.1. ATA Command Set, for a listing of the supported ATA Commands.

8.11. Alternate Status Register

The Alternate Status Register is a read-only register indicating the status of the device, following the previous ATA command. Refer to Section 8.9, Status Register for specific details.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

8.12. Device Control Register

The Device Control Register is used to control the Interrupt Request and issue ATA Software Resets.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write	–	–	–	–	1	SRST	nIEN	0

Notes

Bits 7-4:	Reserved bits.
Bit 3:	Always set to.1
Bit 2: SRST (Software Reset)	When set, resets the ATA software.
Bit 1: nIEN(Interrupt Enable)	When set, device interrupts are disabled. No function in Memory Mapped mode.
Bit 0:	Always set to 0.

8.13. Device Address Register

The Device Address Register is used to maintain compatibility with ATA disk drive interfaces.

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	-	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0
Default Value	0	0	1	1	1	1	1	0

Notes

Bit 7:	Reserved bit.
Bit 6: nWTG (Write Gate)	Low when a write to the device is in process.
Bits 5-2: nHS3 to nHS0	Negated binary address of the currently selected head.
Bit 1: nDS1	Low when Drive 1 is selected and active.
Bit 0: nDS0	Low when Drive 0 is selected and active.

9. ATA COMMAND BLOCK & SET DESCRIPTION

In accordance with the ANSI ATA-3 Specification, the device implements seven registers which are used to transfer instructions to the device by the host. These commands follow the ANSI standard ATA protocol, a description of the ATA Command block is provided below.

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	X							

9.1. ATA Command Set

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	**Check Power Mode**	98h,E5h					D	
1	**Execute Drive Diagnostics**	90h					D	
1	**Erase Sector**	C0h		Y	Y	Y	Y	Y
2	**Format Track**	50h		Y		Y	Y	Y
1	**Identify Drive**	ECh					D	
1	**Idle**	97h,E3h		Y			D	
1	**Idle Immediate**	95h,E1h					D	
1	**Initialize Drive Parameters**	91h		Y			Y	
1	**Read Buffer**	E4h					D	
1	**Read DMA**	C8h		Y	Y	Y	Y	Y
1	**Read Multiple**	C4h		Y	Y	Y	Y	Y
1	**Read Long Sector**	22h,23h			Y	Y	Y	Y
1	**Read Sector(s)**	20h,21h			Y	Y	Y	Y
1	**Read Verify Sector(s)**	40h,41h		Y	Y	Y	Y	Y
1	**Recalibrate**	1Xh					Y	
1	**Request Sense**	03h					D	
1	**Seek**	7Xh			Y	Y	Y	Y
1	**Set Features**	Efh	Y				D	
1	**Set Multiple Mode**	C6h		Y			D	
1	**Set Sleep Mode**	99h,E6h					D	
1	**Standby**	96h,E2h					D	
1	**Standby Immediate**	94h,E0h					D	
1	**Translate Sector**	87h		Y	Y	Y	Y	Y
1	**Wear Level**	F5h					Y	
2	**Write Buffer**	E8h					D	
1	**Write DMA**	CAh		Y	Y	Y	Y	Y
2	**Write Long Sector**	32h,33h			Y	Y	Y	Y
3	**Write Multiple**	C5h		Y	Y	Y	Y	Y
3	**Write Multiple w/o Erase**	CDh		Y	Y	Y	Y	Y
2	**Write Sector(s)**	30h,31h		Y	Y	Y	Y	Y
2	**Write Sector(s) w/o Erase**	38h		Y	Y	Y	Y	Y
3	**Write Verify**	3Ch		Y	Y	Y	Y	Y
–	**NOP**	FFh						

Register Notes: CY - Cylinder; SC - Sector Count; DH – Drive/Head; SN – Sector Number; FR – Feature LBA – LBA bit of the Drive/Head Register ('D' denotes that only the drive bit is used)

9.1.1. Check Power Mode – 98h, E5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	98h or E5h							

The Check Power Mode command verifies the device's current power mode. When the device is configured for standby mode, or is entering or exiting Standby, the BSY bit will be set and the Sector Count register is set to 00h, then clears the BSY bit. In Idle mode, BSY is set and the Sector Count Register is set to FFh, then the BSY bit is cleared and an interrupt is issued.

9.1.2. Executive Drive Diagnostic – 90h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	90h							

The Executive Drive Diagnostic performs an internal read write diagnostic test using (AA55h and 55Aah). If an error is detected in the read/write buffer, the Error Register will report the appropriate Diagnostic Code.

9.1.3. Format Track – 50h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7 – 0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	50h							

The Format Track command formats the common solid-state memory array.

9.1.4. Identify Drive – ECh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	Ech							

Issued by the host, the Identify Drive command provides 256 bytes of Drive attribute data (i.e., Sector Size, Count, etc.) The Identify Drive data structure is detailed in the proceeding table.

9.1.4.1. Identify Drive – Drive Attribute Data

9.1.4.1 Identify Drive – Drive Attribute Data

Word Address	Data Default	Bytes	Data Description
0	044Ah for Fixed ID Bit products (3012, 3021 and others) 848A for Removable ID Bit products (3038, 3005 and others)	2	General Configuration Bit Information 15: Non-magnetic Disk 14: Formatting Speed Latency Permissible Gap needed 13: Track Offset Option supported 12: Data Strobe Offset Option supported 11: Over 0.5% Rotational Speed Difference 10: Disk Transfer Rate > 10Mbps 9: 10Mbps >= Disk Transfer Rate > 5Mbps 8: 5Mbps >= Disk Transfer Rate 7: Removable Cartridge Drive 6: Fixed Drive 5: Spindle Motor Control Option executed 4: Over 15µs Changing Head Time 3: Non-MFM Encoding 2: Soft Sector Allocation 1: Hard Sector Allocation 0: Reserved
1	XXXXh	2	Number of Cylinders
2	0000h	2	Reserved
3	00XXh	2	Number of Heads
4	0000h	2	Number of Unformatted Bytes per Track
5	XXXXh	2	Number of Unformatted Bytes per Sector
6	XXXXh	2	Number of Sectors per Track
7 - 8	XXXXh	4	Number of Sectors per Device
9	0000h	2	Reserved
10 – 19	XXXXh	20	Serial Number
20	0002h	2	Buffer Type 0000h: Not specified 0001h: A single ported single sector buffer 0002h: A dual ported multi-sector buffer 0003h: A dual ported multi-sector buffer with a read caching
21	0002h	2	Buffer Size in 512-byte increments
22	0004h	2	Number of ECC Bytes passed on Read/Write Long Cmds
23 - 26	XXXXh	8	Firmware Revision (8 ASCII Characters)
27 - 46	XXXXh	40	Model Number (40 ASCII Characters)
47	0001h	2	7 – 0: Max Number of Sectors that can be transferred with a Read/Write Multiple Command per Interrupt
48	0000h	2	Double Word (32 bit) not supported
49	0200h	2	9: LBA supported 8: DMA supported
50	0000h	2	Reserved
51	0100h	2	15 – 8: PIO data transfer cycle timing
52	0000h	2	15 – 8: DMA data transfer cycle timing
53	0000h	2	0: Translation Parameters (Word 54 to 58) are valid

9.1.4.1 Identify Drive – Drive Attribute Data

Word Address	Data Default	Bytes	Data Description
54	XXXXh	2	Current Number of Cylinders
55	XXXXh	2	Current Number of Heads
56	XXXXh	2	Current Sectors per Track
57 – 58	XXXXh	4	Current Capacity in Sectors
59	010Xh	2	7 – 0: Current Sectors can be transferred with a Read/Write Multiple command per interrupt
60 - 61	XXXXh	4	Total Number of Sectors addressable in LBA Mode
62	0000h	2	Single-word DMA Modes supported
63	0407h	2	Multi-word DMA Modes supported
64	0003h	2	PIO Modes supported
65	0078h	2	Minimum DMA transfer cycle time per word (ns)
66	0078h	2	Manufacturer's recommended DMA transfer cycle time (ns)
67	0078h	2	Minimum PIO transfer cycle time without flow control (ns)
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow controls (ns)
69-127	0000h	118	Reserved
128 – 159	0000h	64	Vendor Unique
160 - 255	0000h	192	Reserved

9.1.5. Idle – 97h, E3h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Timer Count (5ms increments)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	97h or E3h							

When issued by the host, the device's internal controller sets the BSY bit, enters the Idle mode, clears the BSY bit, and generates an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is disabled.

9.1.6. Idle Immediate – 95h, E1h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	95h or E1h							

When issued by the host the device's internal controller sets the BSY bit, enters Idle Mode, clears the BSY bit, and issues an interrupt. The interrupt is issued whether or not the Idle mode is fully entered.

9.1.7. Initialize Drive Parameters – 91h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count (Number of Sectors)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	0	X	Drive	Head Number (Number of Heads – 1)			
Command	91h							

Initialize Drive Parameters allows the host to set the sector counts per track and the head counts per cylinder to "1" fixed. Upon issuance of the command the device will set the BSY bit and associated parameters, clears the BSY bit and issues an interrupt.

9.1.8. Recalibrate – 1Xh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	1Xh							

The Recalibrate command sets the Cylinder Low & High, and the Head Number to “0h”, and Sector Number to “1h” in CHS mode. In LBA mode (i.e., LBA = 1) the Sector Number is set to “0h”.

9.1.9. Read Buffer – E4h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E4h							

This command allows the host to read the contents of the sector buffer. When issued the device sets the BSY bit and sets up the sector buffer data in preparation for the read operation. Once the data is ready, the DRQ bit is set and the BSY bit in the status register are set and cleared, respectively.

9.1.10. Read DMA – C8h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C8h							

This command allows the host to read data using the DMA transfer protocol.

9.1.11. Read Multiple – C4h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C4h							

This command executes similarly to the Read Sector command with the exception that, interrupts are issued only when a block containing the counts of sectors defined by the Set Multiple command is transferred.

9.1.12. Read Sector – 20h, 21h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	20h or 21h							

The Read Sector command allows the host to read sectors 1 to 256 as specified in the Sector Count Register. If the Sector count is set to “0h”, all 256 Sectors of data will be made available. Once the command code is issued and the first sector of data has been transferred to the buffer the DRQ bit will be set. The Read Sector command is terminated by writing the cylinder, head, and sector number of the last sector read in the task file. On error, the read operation is aborted in the errant sector.

9.1.13. Read Long Sector(s) – 22h, 23h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	22h or 23h							

The Read Long Sector(s) command operates similarly to the Read Sector(s) command, with the exception that is transfers requested data sectors and ECC data. The long instruction ECC byte transfer for Long commands is a byte transfer at a fixed length of 4 bytes.

9.1.14. Read Verify Sector(s) – 40h, 41h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	40h or 41h							

The Read Verify Sector(s) command operates similarly to the Read Sector(s) command, with the exception that is does not set the DRQ bit and does not transfer data to the host. One the requested sectors have been verified, the onboard controller clears the BSY bit and issues an interrupt.

9.1.15. Seek – 7Xh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	7Xh							

The Seek command seeks and picks up the head to tracks specified in the task file. When the command is issued, the Solid-state memory chips need not be formatted. After an appropriate amount of time the DSC bit is set.

9.1.16. Set Features – EFh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	Feature							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	EFh							

9.1.16. Set Features – EFh (*continued)*

This command allows the host to configure the Feature Set of the device according to the attributes listed below.

Feature	Operation
01h	Enable 8 bit Data Transfer
66h	Disable Reverting to Power On Defaults
81h	Disable 8 bit Data Transfer
BBh	4 Bytes of Data Apply on Read/Write Long Commands
CCh	Enable revert to Power on Defaults

On Power-up or following a Hardware Reset, the device will be set to the default mode “81h”.

9.1.17. Set Multiple Mode – C6h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	C6h							

The Set Multiple Mode command allows the host to access the drive via Read Multiple and Write Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple command. The sector count per block is set in the Sector Count register.

9.1.18. Set Sleep Mode – 99h, E6h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	99h or E6h							

The Set Sleep Mode command allows the host to set the device in Sleep mode. When the onboard controller transitions to Sleep mode, it clears the BSY bit and issues an interrupt, and the device interface becomes inactive. Sleep mode can be exited by issuing either a hardware or software reset.

9.1.19. Standby – 96h, E2h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Timer Count(5msec x Timer Count)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	96h or E2h							

The Standby command, when issued by the host will transition the device into the Standby mode. If the Sector Count Register is set to a value other than “0h”, the Auto Power Down function is enabled and the device will return to Idle mode.

9.1.20. Standby Immediate – 94h, E0h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	94h or E0h							

The Standby Immediate command, when issued by the host will transition the device into the Standby mode.

9.1.21. Write Buffer – E8h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E8h							

The Write Buffer command allows the host to rewrite the contents of the 512 byte data buffer with the desired data.

9.1.22. Write DMA – CAh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	CAh							

The Write DMA command allows the host to write data using the DMA transfer protocol.

9.1.23. Write Multiple – C5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	C5h							

The Write Multiple command operates in the same manner as the Write Sector command, when issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

9.1.24. Write Sector(s) – 30h, 31h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	30h or 31h							

The Write Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count Register. A Sector count of 0 requests 256 Sectors. When issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

9.1.25. Write Long Sector(s) – 32h, 33h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	32h or 33h							

The Write Long Sector(s) command operates in the same manner as the Write Sector command, when issued the device will set the BSY bit within 400nsec, an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

9.1.26. Erase Sector(s) – C0h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	C0h							

The Erase Sector(s) command is issued prior to the issuance of a Write Sector(s) or Write Multiple w/o Erase command.

9.1.27. Request Sense – 03h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	X	1	Drive	X			
Command	03h							

The Request Sense command identifies the Extended Error Codes generated by the preceding ATA command. The Request Sense command must be issued immediately following the detection of an error via the Error Register.

Extended Error Codes	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or Generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30h-32h, 37h,3Eh	Self Test of Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error/ Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Computed Media Format
03h	Write/Erase Failed

9.1.28. Translate Sector – 87h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	87h							

The Translate Sector command is not currently supported by the SiliconSystems SiliconDrive PC. If the host issues this command the device will respond with 0x00h in the data register.

9.1.29. Wear Level – F5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Completion Status							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	Flag			
Command	F5h							

The Wear Level command is supported as a NOP command for the purposes of backward compatibility with the ANSI AT Attachment Standard. This command sets the Sector Count Register to 0x00h after processing this command.

9.1.30. Write Multiple w/o Erase – CDh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	CDh							

The Write Multiple w/o Erase command functions identically to the Write Multiple command with the exception that the implied pre-erase (i.e., Erase Sector(s) Command) is not issued prior to writing the sectors.

9.1.31. Write Sector(s) w/o Erase – 38h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	38h							

The Write Sector(s) w/o Erase command functions similar to the Write Sector command, however the implied pre-erase (i.e., Erase Sector(s) Command) is not issued prior to writing the sectors.

9.1.32. Write Verify – 3Ch

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	3Ch							

The Write Verify command verifies each sector immediately after it is written. This command performs identically to the Write Sector(s) command with the added feature of verifying each sector written.

9. SALES AND SUPPORT

To order or to obtain information on pricing and delivery, please contact your SiliconSystems Sales Representative.

10.1. Part Numbering Nomenclature

The following table defines the SiliconDrive PC part numbering scheme:

Definition						
SSD-	P	YYY	T	-XXXX		
				SiliconSystems Proprietary		
			Temp. Range: Blank=Commercial, I=Industrial			
		Capacity: 16G=16GB / 32=32M				
	Form Factor: P = PC Card					
SiliconSystems SiliconDrive						
Operating Temperature Range: Commercial: 0°C to 70°C, Industrial: -40°C to +85°C						

Part Number	Description
SSD-P16G-3100	16GB SiliconDrive PC, Commercial Temp
SSD-P08G-3100	8GB SiliconDrive PC, Commercial Temp
SSD-P06G-3100	6GB SiliconDrive PC, Commercial Temp
SSD-P04G-3100	4GB SiliconDrive PC, Commercial Temp
SSD-P02G-3100	2GB SiliconDrive PC, Commercial Temp
SSD-P01G-3100	1GB SiliconDrive PC, Commercial Temp
SSD-P51M-3100	512MB SiliconDrive PC, Commercial Temp
SSD-P25M-3100	256MB SiliconDrive PC, Commercial Temp
SSD-P12M-3100	128MB SiliconDrive PC, Commercial Temp
SSD-P64M-3100	64MB SiliconDrive PC, Commercial Temp
SSD-P32M-3100	32MB SiliconDrive PC, Commercial Temp

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